

# Compal Confidential

## ICL50/51, ICK70/71 Schematics Document

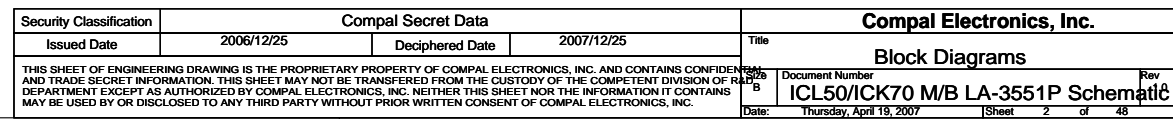
Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M  
(With ATI MXM/B)

2007-4-20

REV: 1A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/04/04	Deciphered Date	2008/04/04	Title	Cover Page
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				ICL50/ICK70 M/B LA-3551	Schematic
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**Model Name : ICL50/51, ICK70/ICK71**  
**File Name : LA-3551P**



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

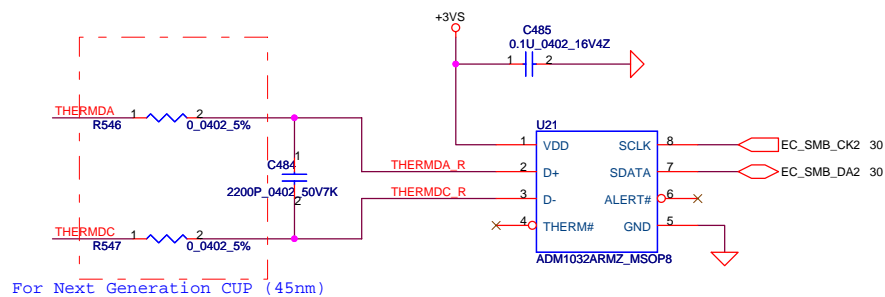
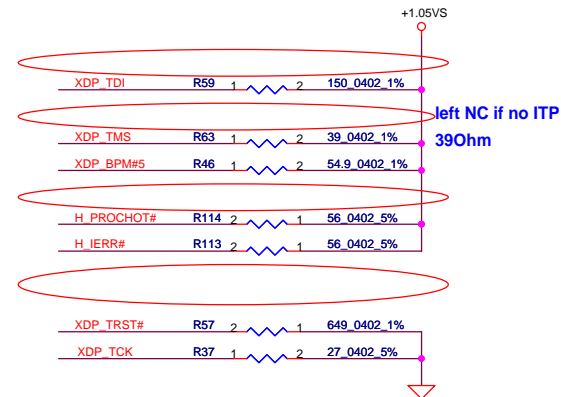
BTO Item	BOM Structure
Discrete	PM@
UMA	GM@



Merom Ball-out Rev 1a  
CONN@

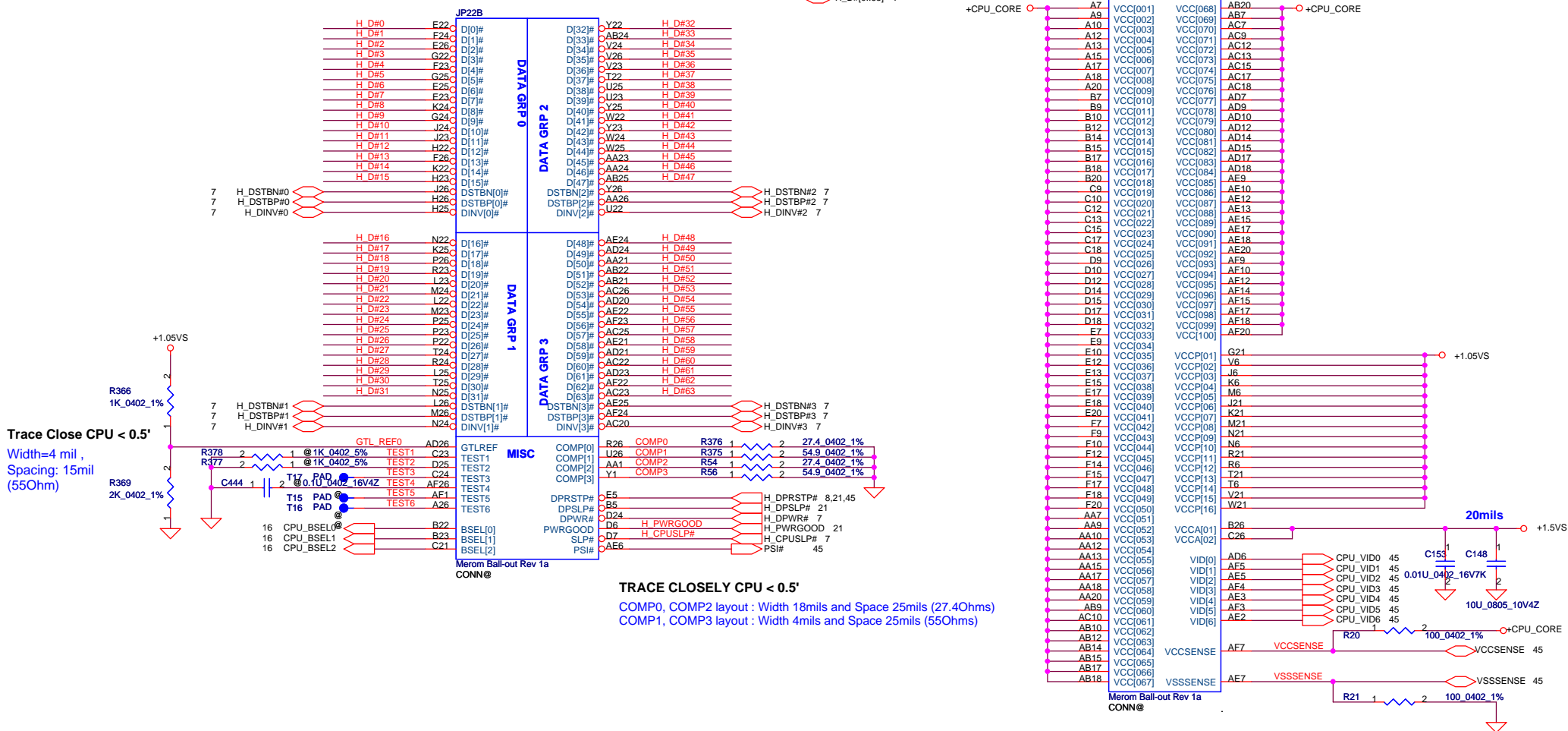
BSEL2	BSEL1	BSEL0	BCLK
0	1	0	200
0	1	1	166

Layout Note:  
THERMDA&THERMDC Trace / Space = 10 / 10 mil  
THERMDA\_R&THERMDC\_R Trace / Space = 10 / 10 mil



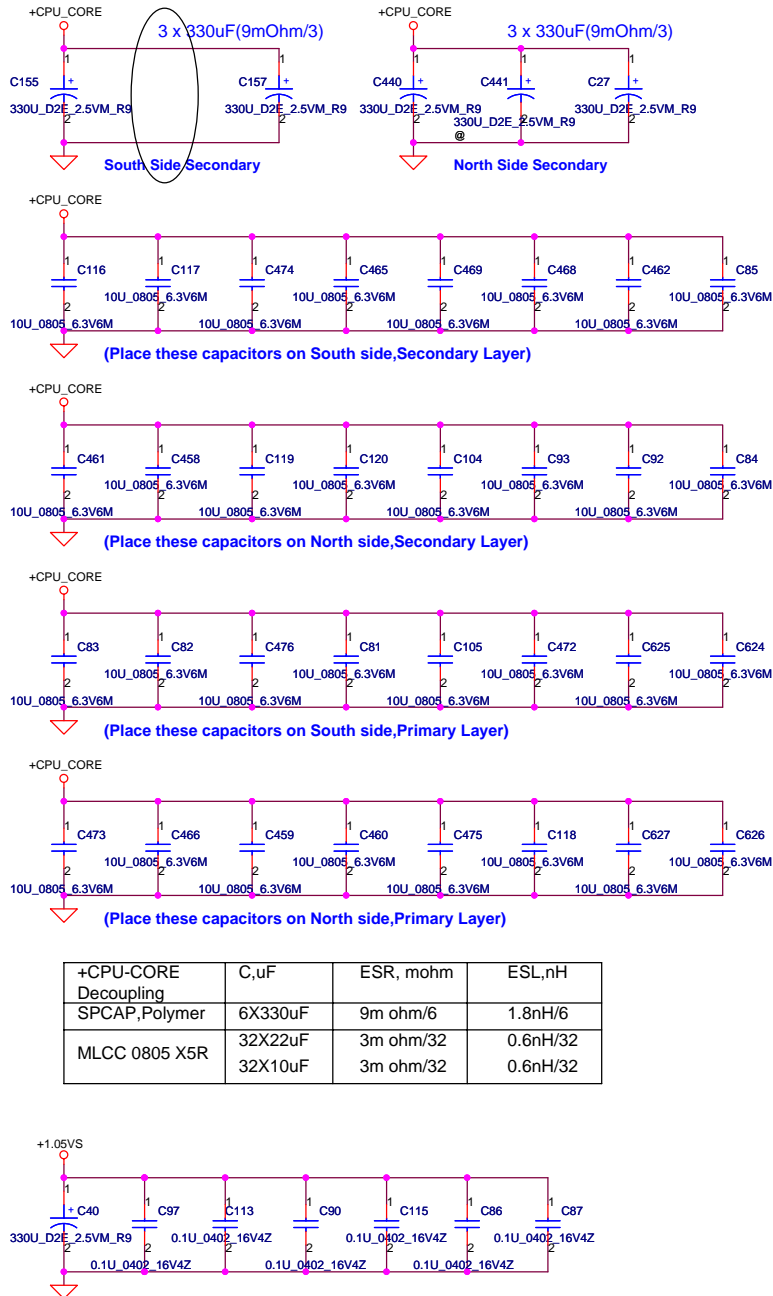
For Next Generation CUP (45nm)

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Date		Monday, April 23, 2007		Document Number	ICL50/ICK70 M/B LA-3551P Schematic
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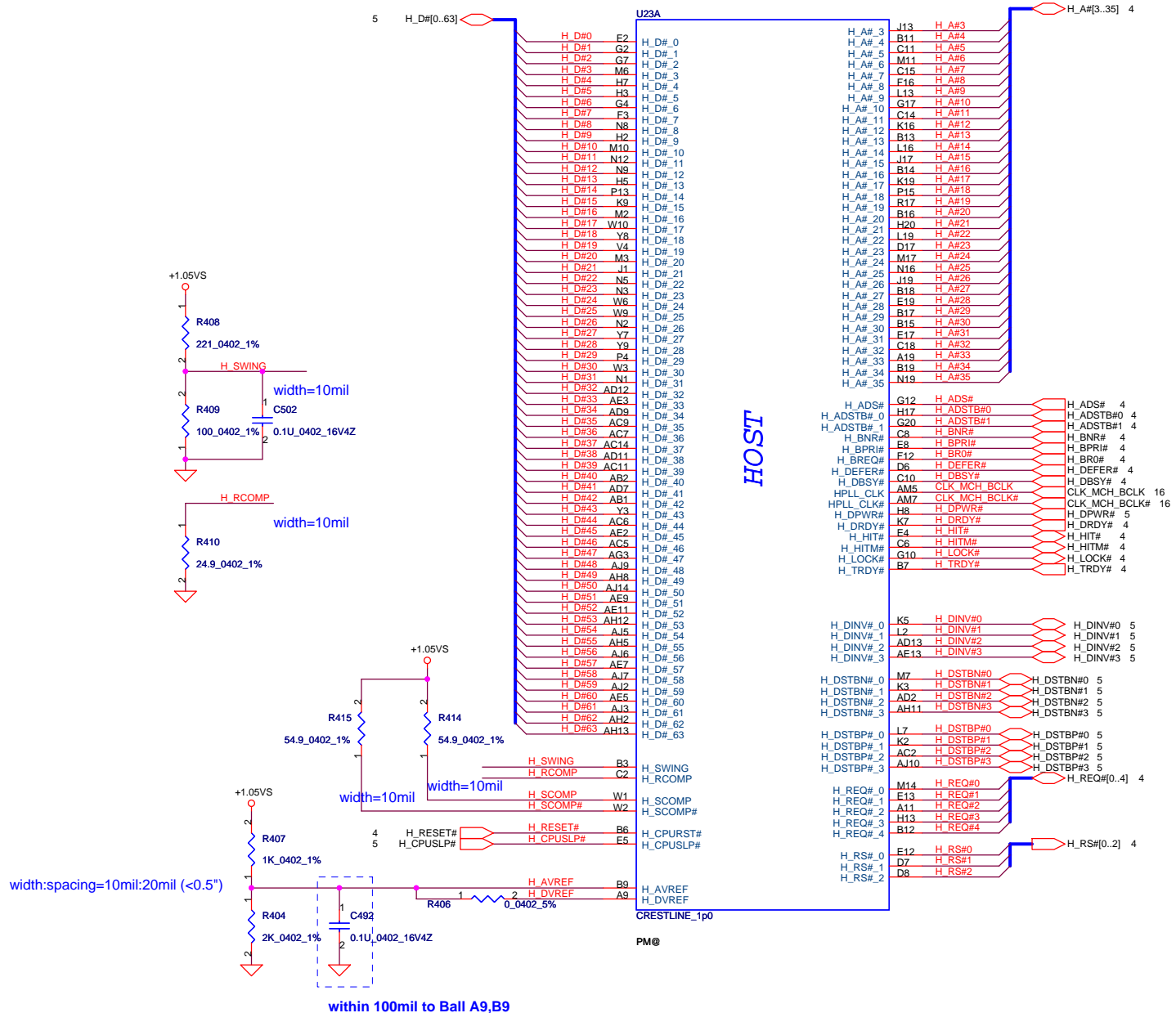


JP22D	
A4	VSS[001]
A8	VSS[002]
A11	VSS[003]
A14	VSS[004]
A16	VSS[005]
A19	VSS[006]
A23	VSS[007]
AF2	VSS[008]
B6	VSS[009]
B8	VSS[010]
B11	VSS[011]
B13	VSS[012]
B16	VSS[013]
B19	VSS[014]
B21	VSS[015]
B24	VSS[016]
C5	VSS[017]
C8	VSS[018]
C11	VSS[019]
C14	VSS[020]
C16	VSS[021]
C19	VSS[022]
C2	VSS[023]
C22	VSS[024]
C25	VSS[025]
D1	VSS[026]
D4	VSS[027]
D8	VSS[028]
D11	VSS[029]
D16	VSS[030]
D19	VSS[031]
D23	VSS[032]
D26	VSS[033]
E3	VSS[034]
E6	VSS[035]
E8	VSS[036]
E11	VSS[037]
E14	VSS[038]
E16	VSS[039]
E19	VSS[040]
E21	VSS[041]
E24	VSS[042]
F5	VSS[043]
F8	VSS[044]
F11	VSS[045]
F13	VSS[046]
F16	VSS[047]
F19	VSS[048]
F2	VSS[049]
F22	VSS[050]
F25	VSS[051]
G4	VSS[052]
G1	VSS[053]
G23	VSS[054]
G26	VSS[055]
H3	VSS[056]
H6	VSS[057]
H21	VSS[058]
H24	VSS[059]
J2	VSS[060]
J5	VSS[061]
J22	VSS[062]
J25	VSS[063]
K1	VSS[064]
K4	VSS[065]
K23	VSS[066]
K26	VSS[067]
L3	VSS[068]
L6	VSS[069]
L21	VSS[070]
L24	VSS[071]
M2	VSS[072]
M5	VSS[073]
M22	VSS[074]
M25	VSS[075]
N1	VSS[076]
N4	VSS[077]
N23	VSS[078]
N26	VSS[079]
P3	VSS[080]
	VSS[081]
	VSS[082]
	VSS[083]
	VSS[084]
	VSS[085]
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	VSS[162]
	VSS[163]

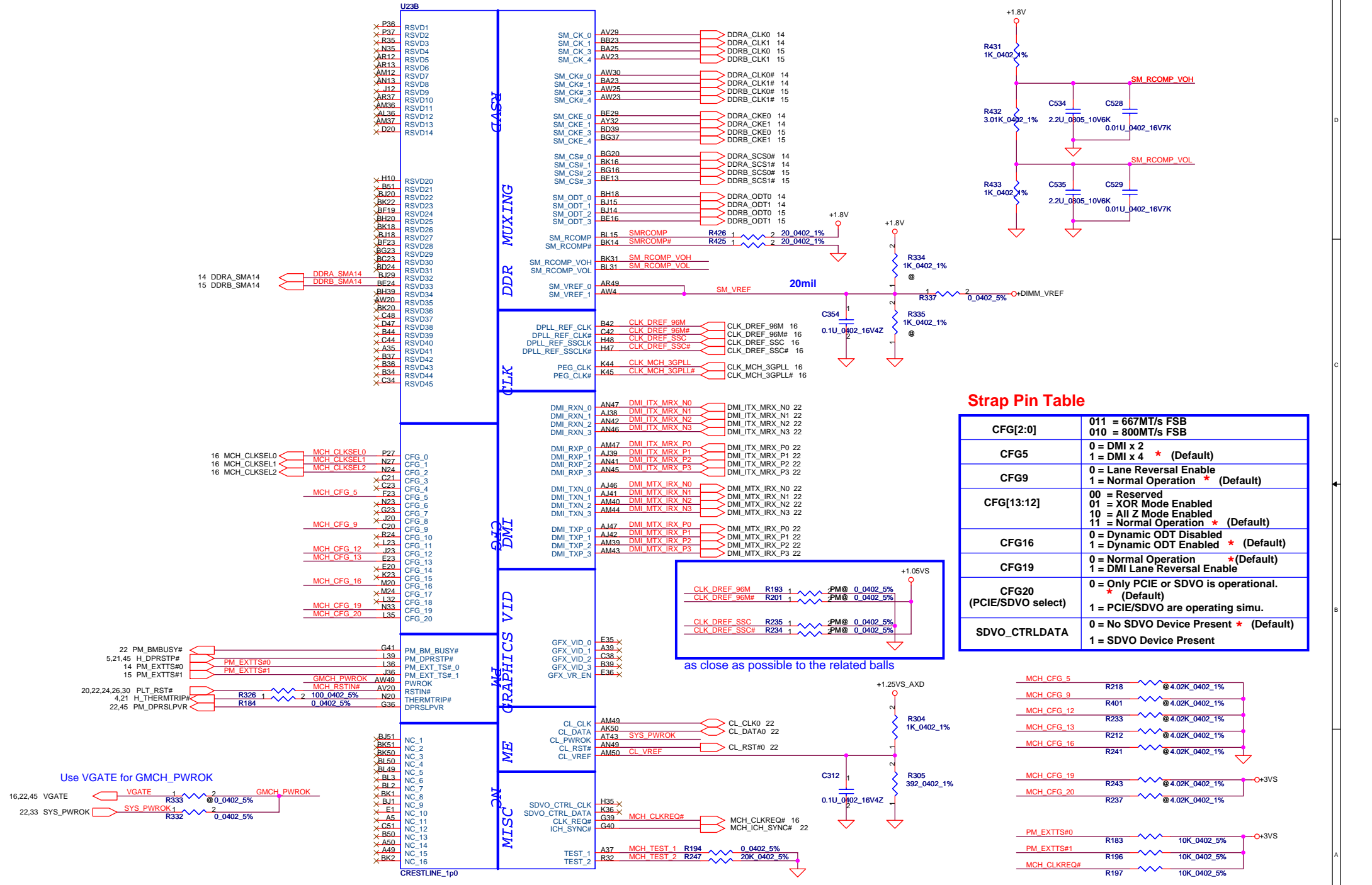
Merom Ball-out Rev 1a  
CONN@



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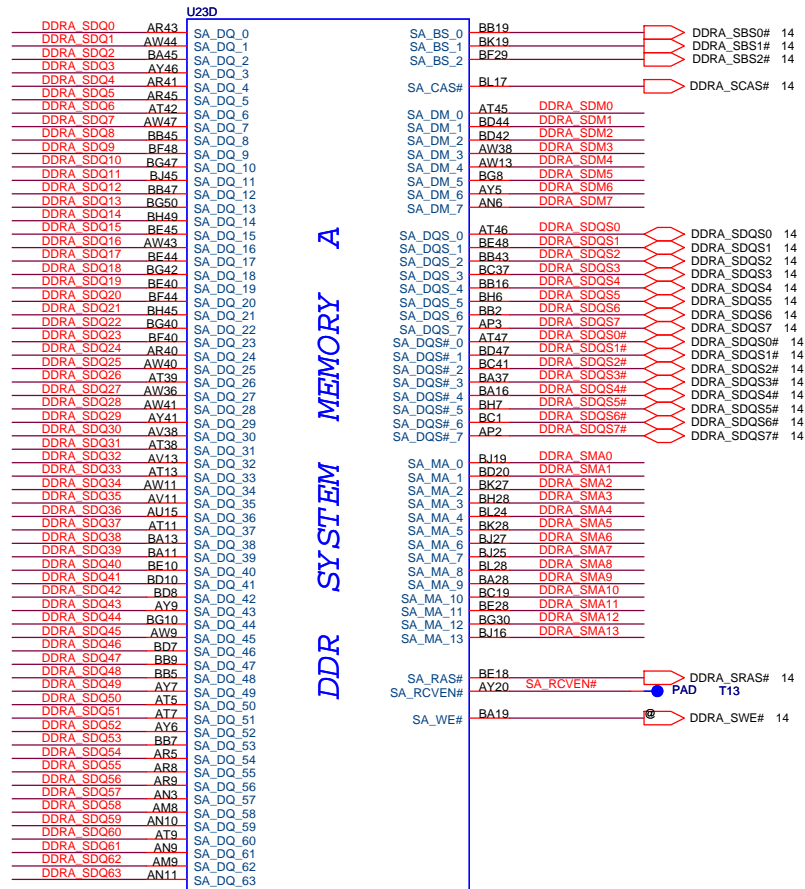
Strap Pin Table

CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present



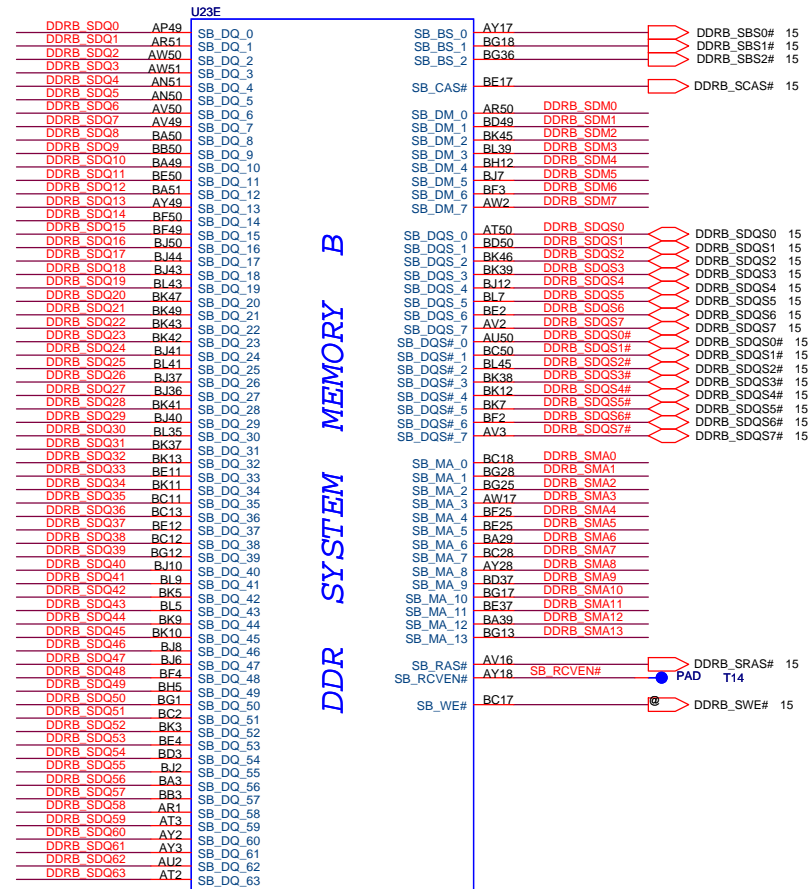
14 DDRA\_SDQ[0..63] DDRA\_SDQ[0..63]  
14 DDRA\_SDM[0..7] DDRA\_SDM[0..7]  
14 DDRA\_SMA[0..13] DDRA\_SMA[0..13]

15 DDRB\_SDQ[0..63] DDRB\_SDQ[0..63]  
15 DDRB\_SDM[0..7] DDRB\_SDM[0..7]  
15 DDRB\_SMA[0..13] DDRB\_SMA[0..13]



CRESTLINE\_1p0

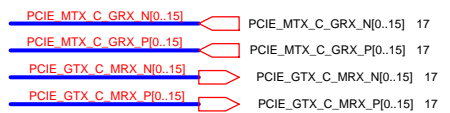
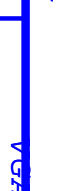
PM@



CRESTLINE\_1p0

PM@

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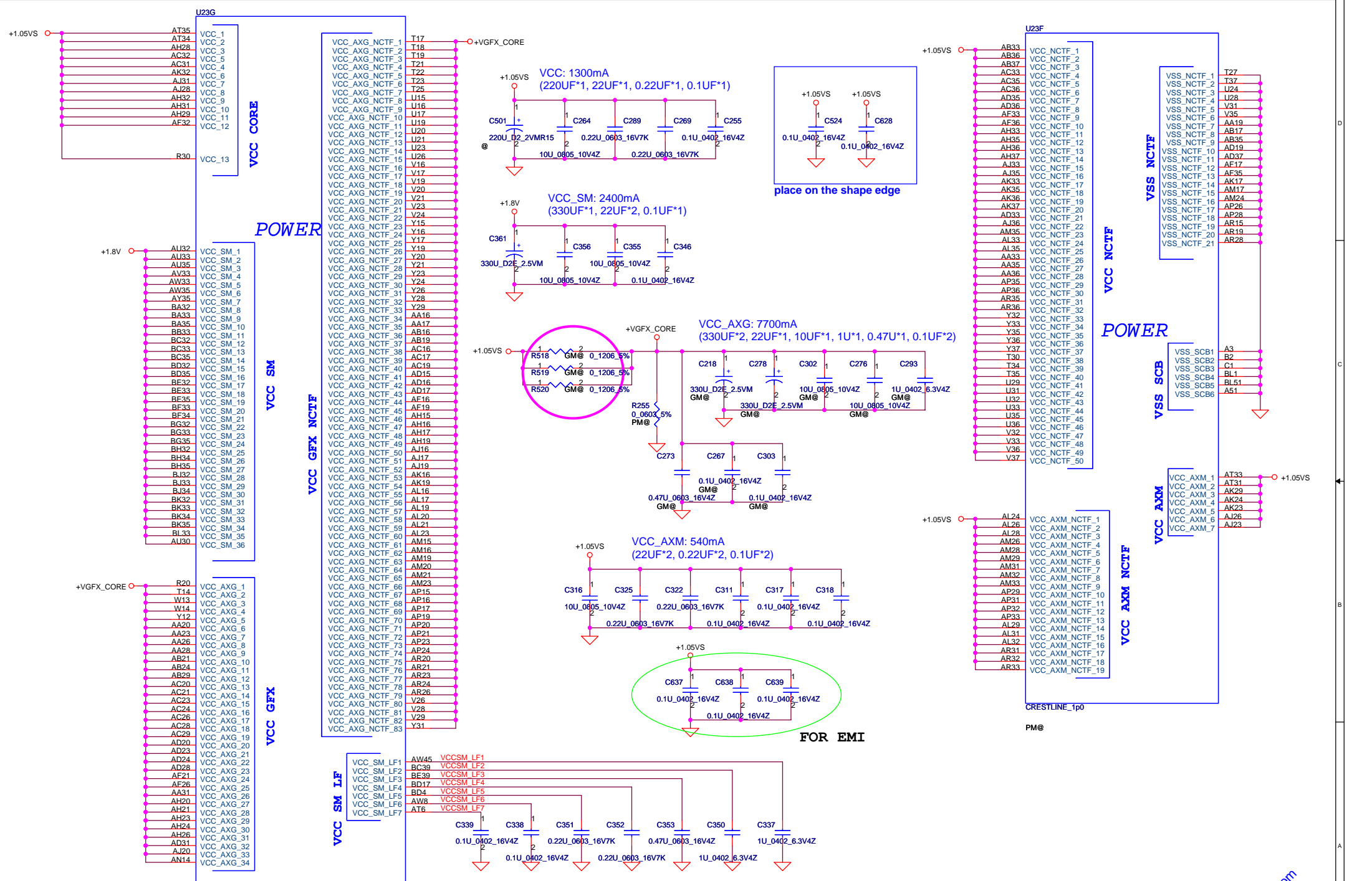
PCIE_MTX_C_GRX_N[0..15]	PCIE_MTX_C_GRX_N[0..15]	17
PCIE_MTX_C_GRX_P[0..15]	PCIE_MTX_C_GRX_P[0..15]	17
PCIE_GTX_C_MRX_N[0..15]	PCIE_GTX_C_MRX_N[0..15]	17
PCIE_GTX_C_MRX_P[0..15]	PCIE_GTX_C_MRX_P[0..15]	17

PCIE_MTX_C_GRX_N[0..15]	PCIE_MTX_C_GRX_N[0..15]	17
PCIE_MTX_C_GRX_P[0..15]	PCIE_MTX_C_GRX_P[0..15]	17
PCIE_GTX_C_MRX_N[0..15]	PCIE_GTX_C_MRX_N[0..15]	17
PCIE_GTX_C_MRX_P[0..15]	PCIE_GTX_C_MRX_P[0..15]	17

		C179		2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N0
1	2	PM@ 0.1U_0402_16V7K	C185	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N1
1	2	PM@ 0.1U_0402_16V7K	C212	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N2
1	2	PM@ 0.1U_0402_16V7K	C229	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N3
1	2	PM@ 0.1U_0402_16V7K	C246	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N4
1	2	PM@ 0.1U_0402_16V7K	C261	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N5
1	2	PM@ 0.1U_0402_16V7K	C277	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N6
1	2	PM@ 0.1U_0402_16V7K	C296	2	PM@ 0.1U_0402_16V7K	PCIE MTX C GRX N7
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N8
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N9
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N10
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N11
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N12
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N13
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N14
1	2	PM@ 0.1U_0402_16V7K				PCIE MTX C GRX N15

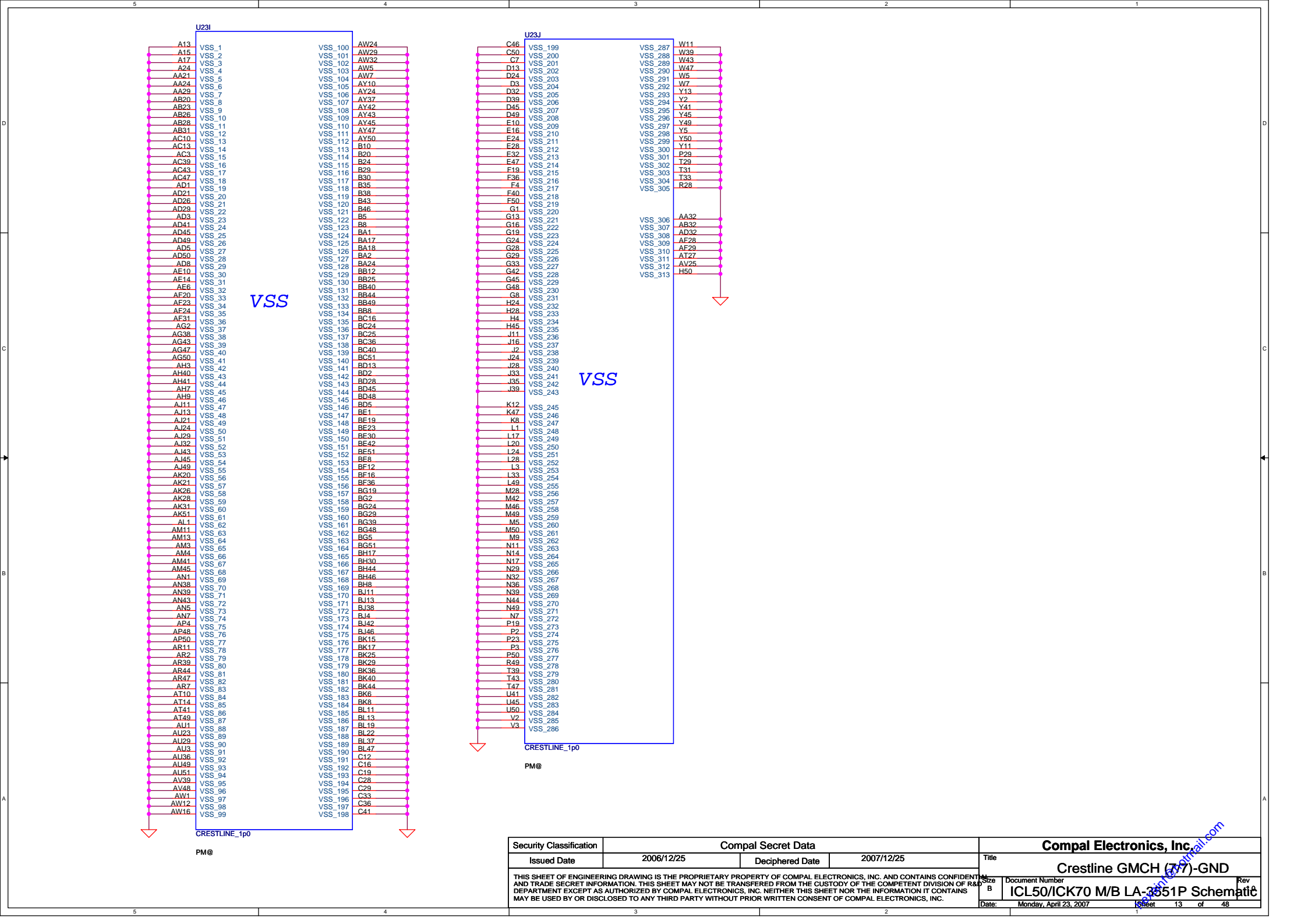
1			C176	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P0
1	2	PM@ 0.1U_0402 16V7K	C189	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P1
1	2	PM@ 0.1U_0402 16V7K	C204	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P2
1	2	PM@ 0.1U_0402 16V7K	C219	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P3
1	2	PM@ 0.1U_0402 16V7K	C241	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P4
1	2	PM@ 0.1U_0402 16V7K	C253	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P5
1	2	PM@ 0.1U_0402 16V7K	C272	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P6
1	2	PM@ 0.1U_0402 16V7K	C288	1	2	PM@ 0.1U_0402 16V7K	PCIE MTX C GRX P7
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P8
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P9
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P10
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P11
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P12
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P13
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P14
1	2	PM@ 0.1U_0402 16V7K					PCIE MTX C GRX P15

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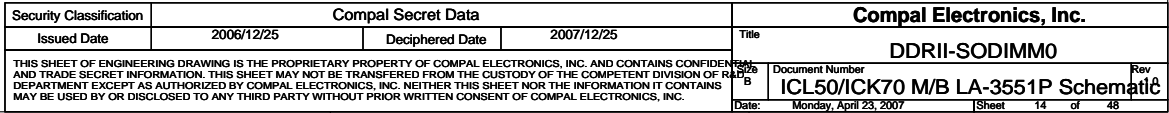


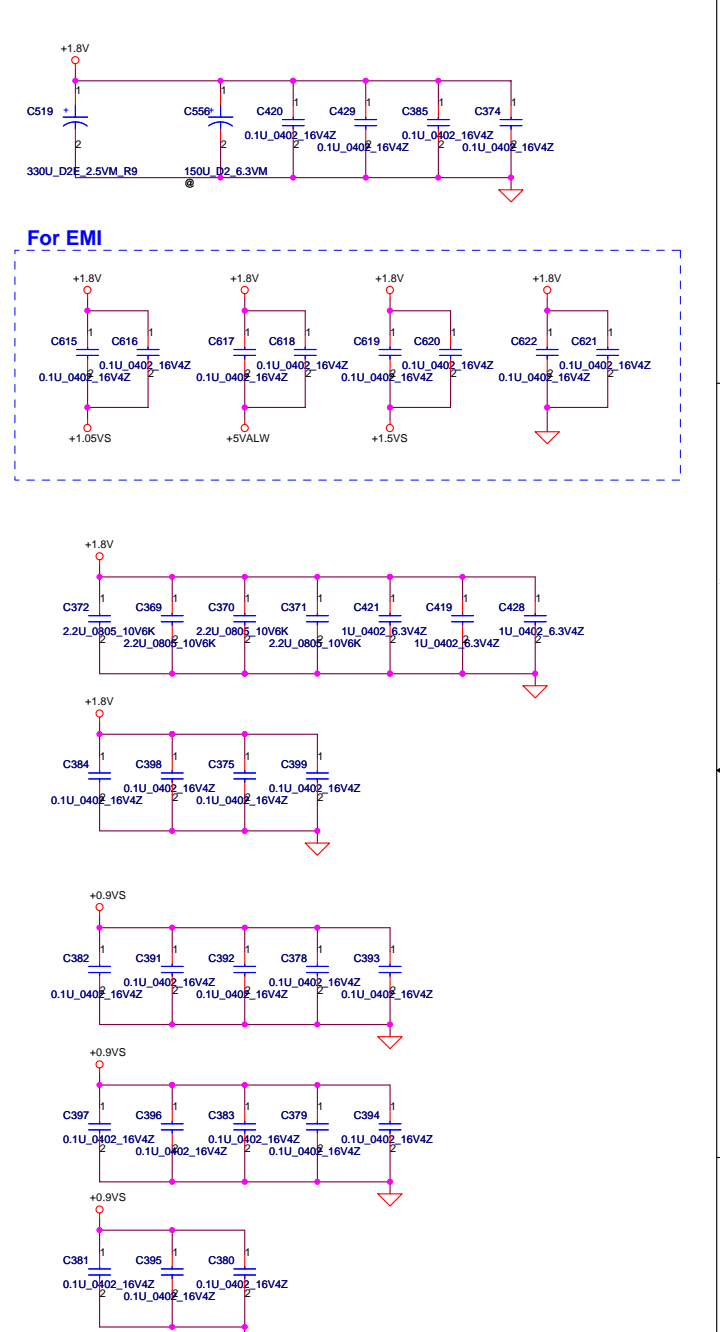
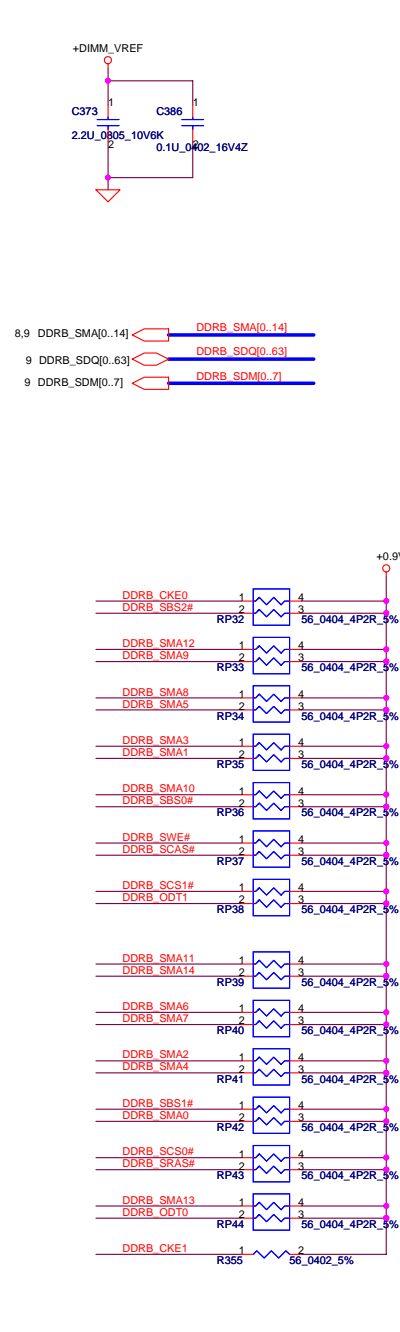
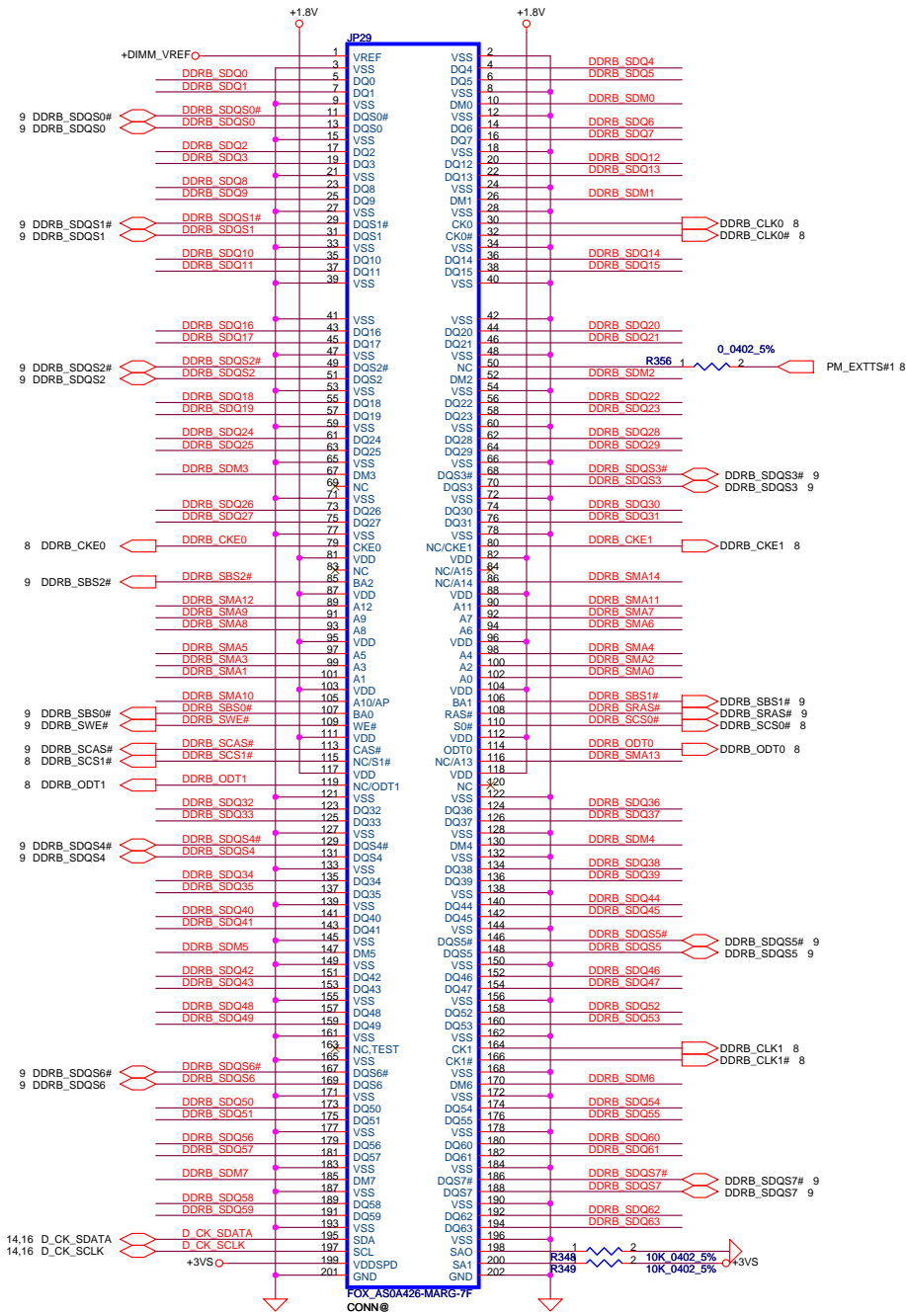
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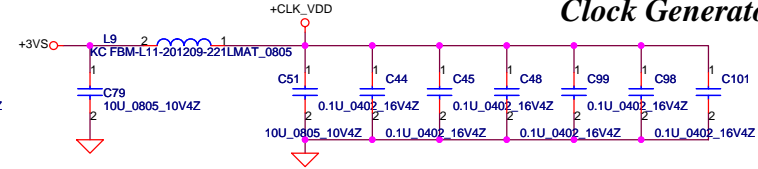
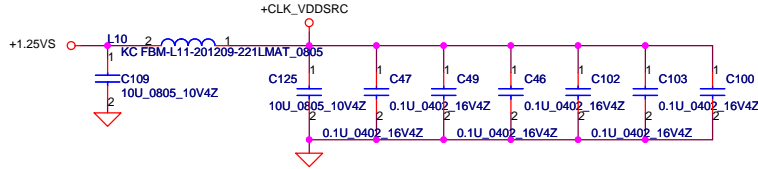
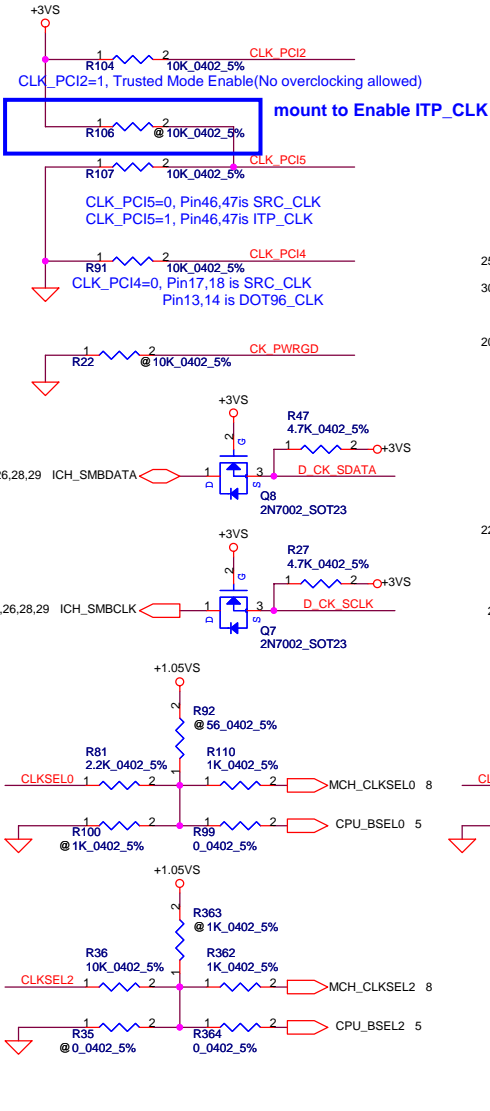


FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR365

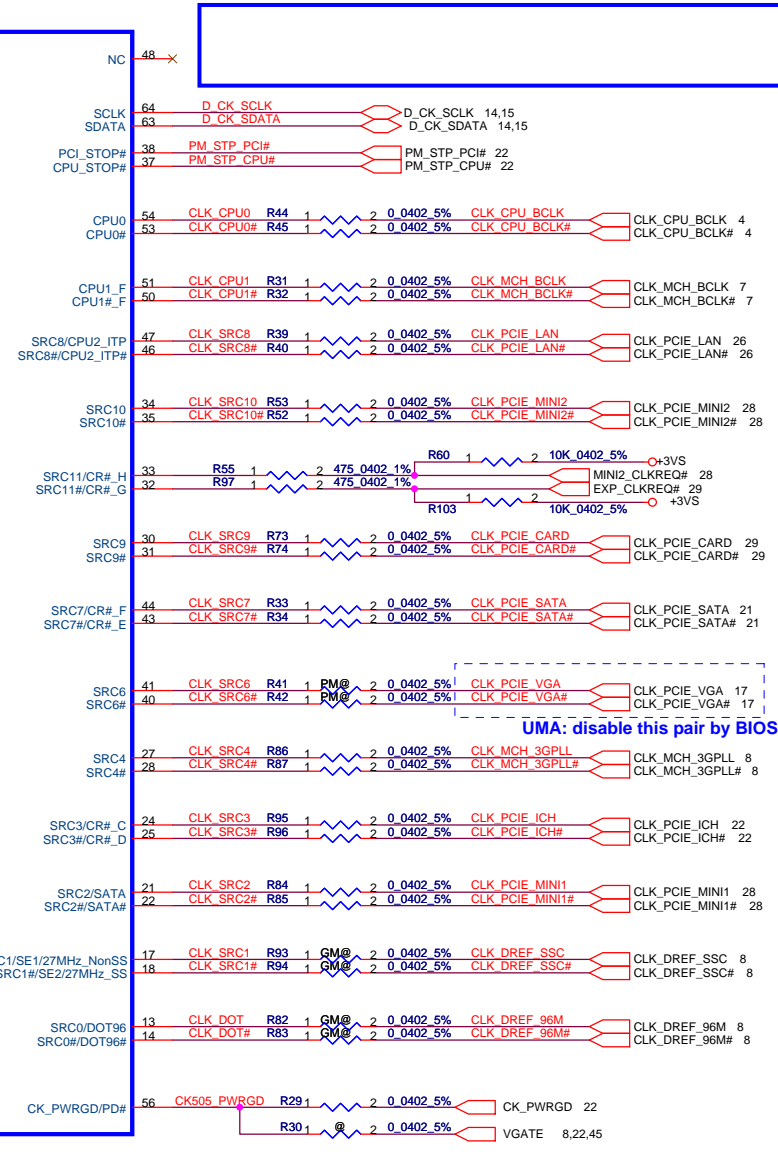
CLK_REQ#	Control	Free-Run
CR#_A(WLAN)	PCIEX2	PCIEX0
CR#_B(MCH)	PCIEX4	PCIEX1
CR#_G(NEW CARD)	PCIEX9	
CR#_H(MINI CARDII)	PCIEX10	

SRC6(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



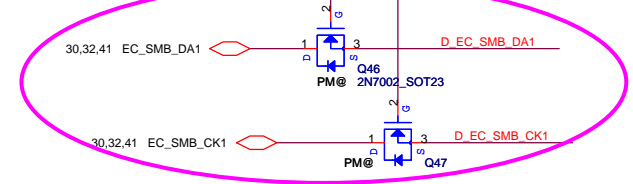
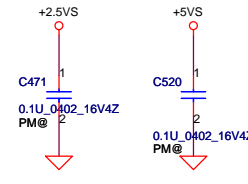
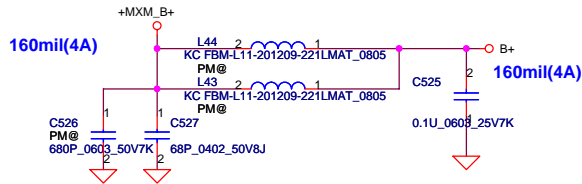
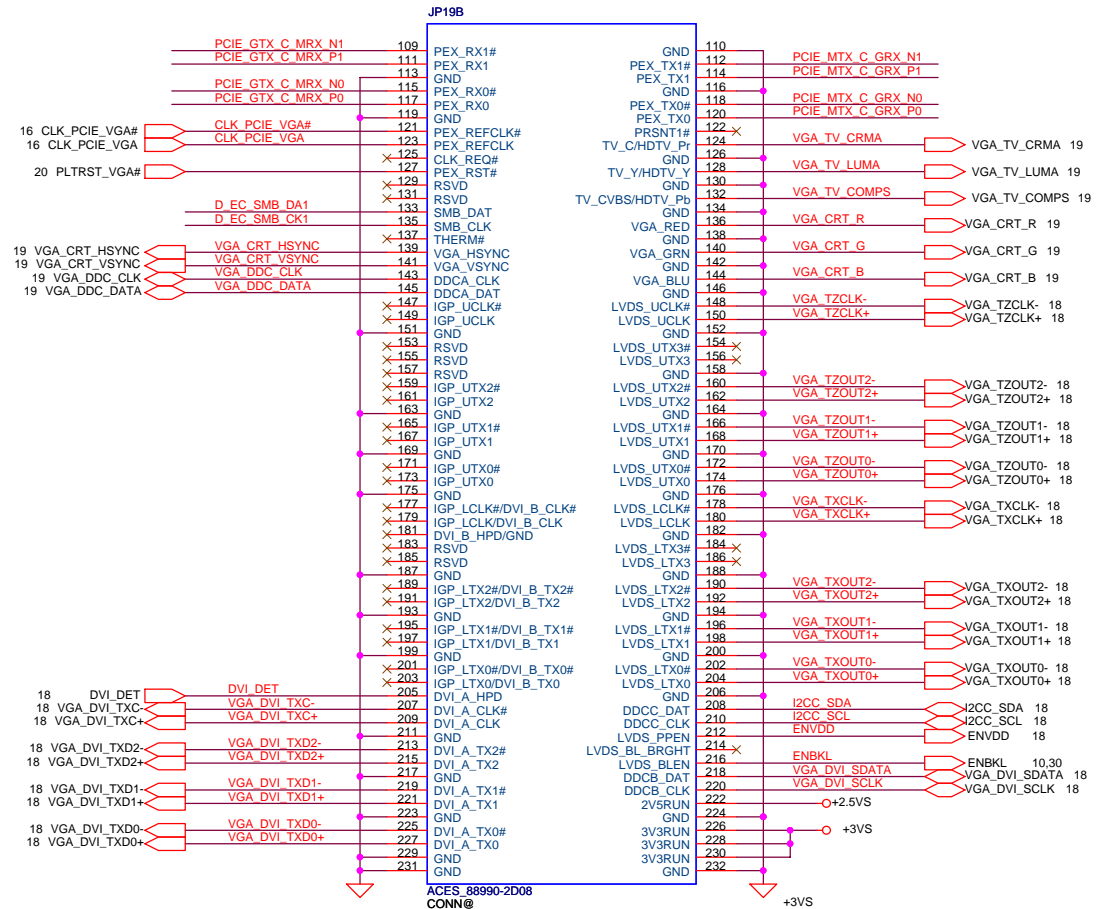
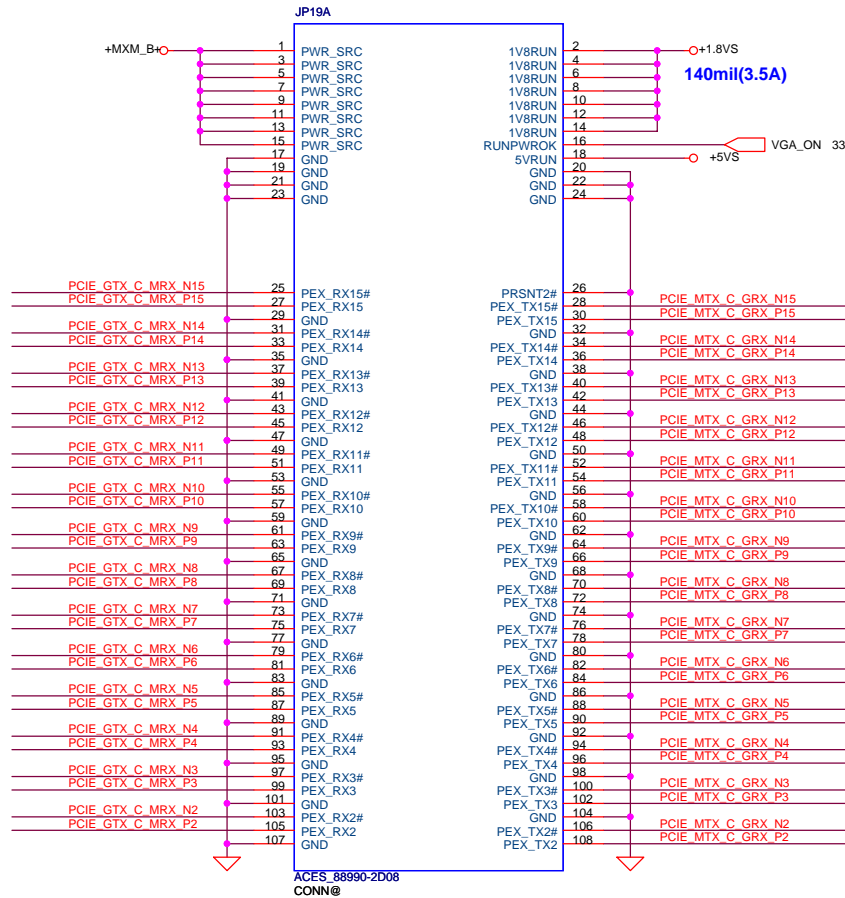
## Clock Generator

mount to Enable ITP\_CLK



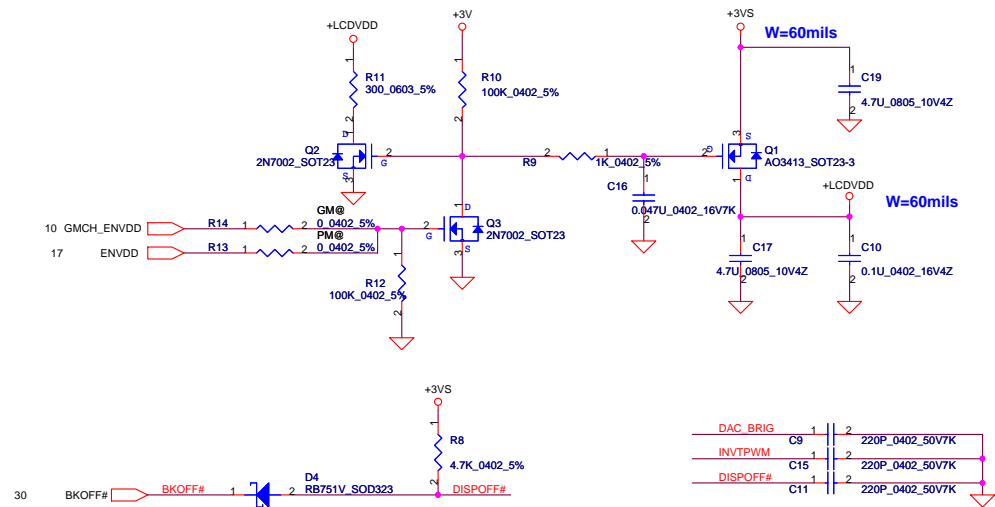
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				ICL50/ICK70 M/B LA-3551P Schematic	
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10 PCIE\_MTX\_C\_GRX\_N[0..15] PCIE\_MTX\_C\_GRX\_P[0..15]  
10 PCIE\_MTX\_C\_GRX\_P[0..15] PCIE\_MTX\_C\_GRX\_P[0..15]  
10 PCIE\_GTX\_C\_MRX\_N[0..15] PCIE\_GTX\_C\_MRX\_P[0..15]  
10 PCIE\_GTX\_C\_MRX\_P[0..15] PCIE\_GTX\_C\_MRX\_P[0..15]

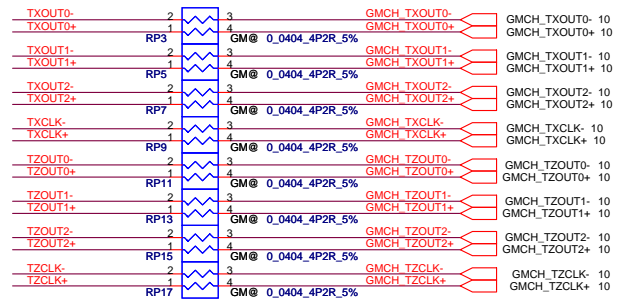
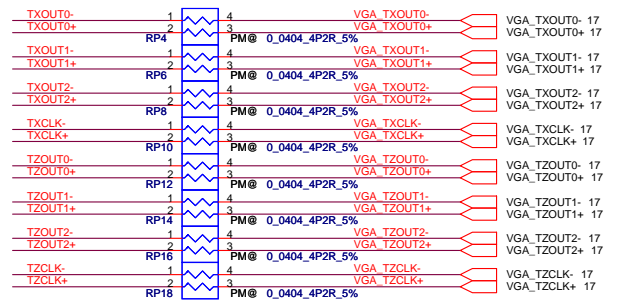
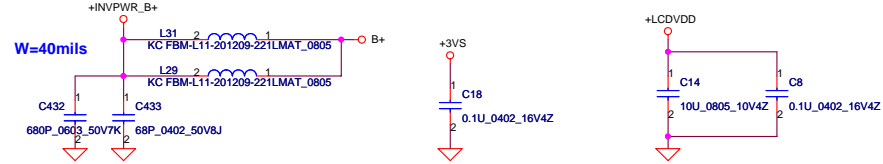
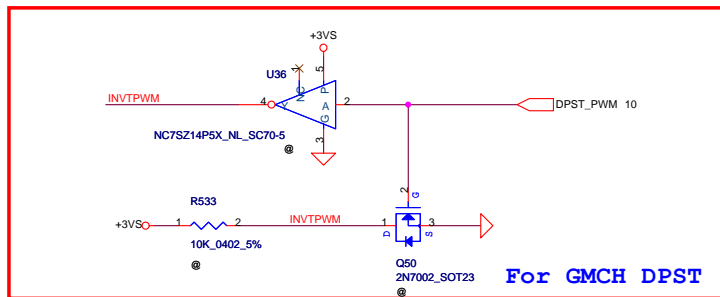
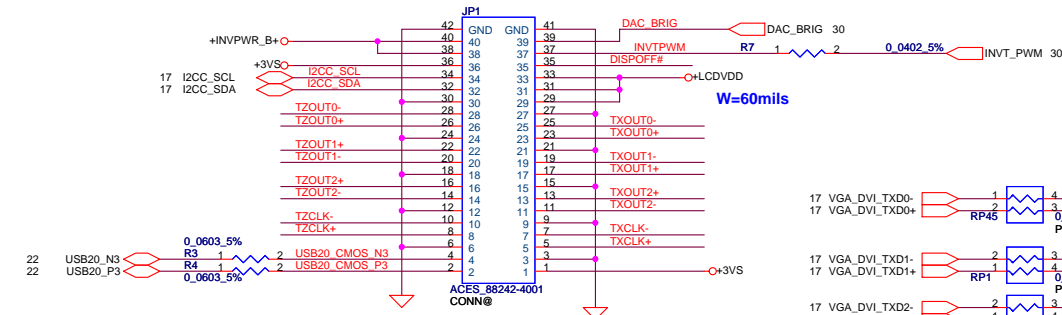


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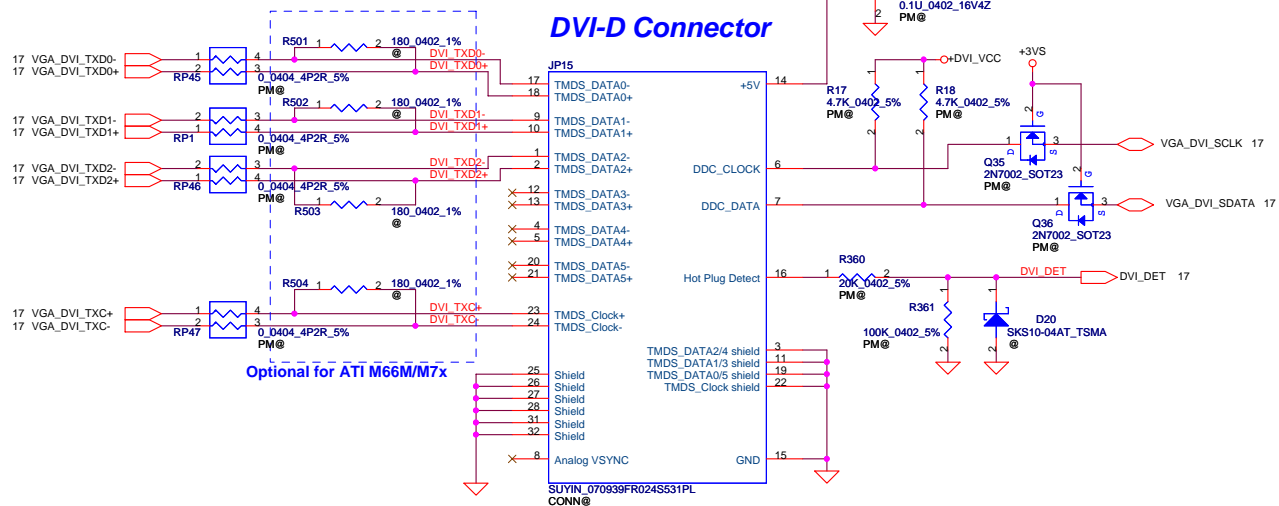
## LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.

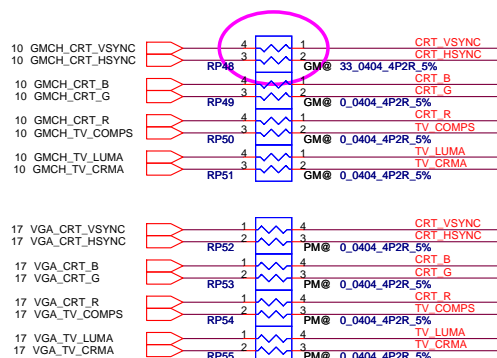


## DVI-D Connector



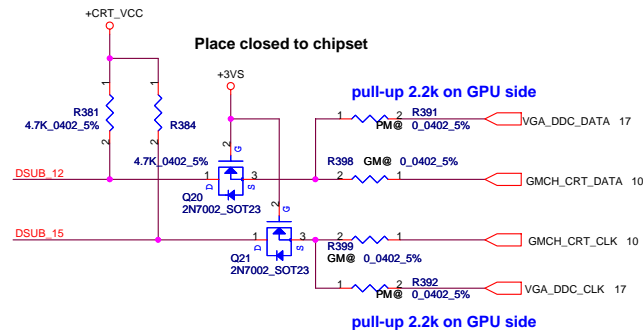
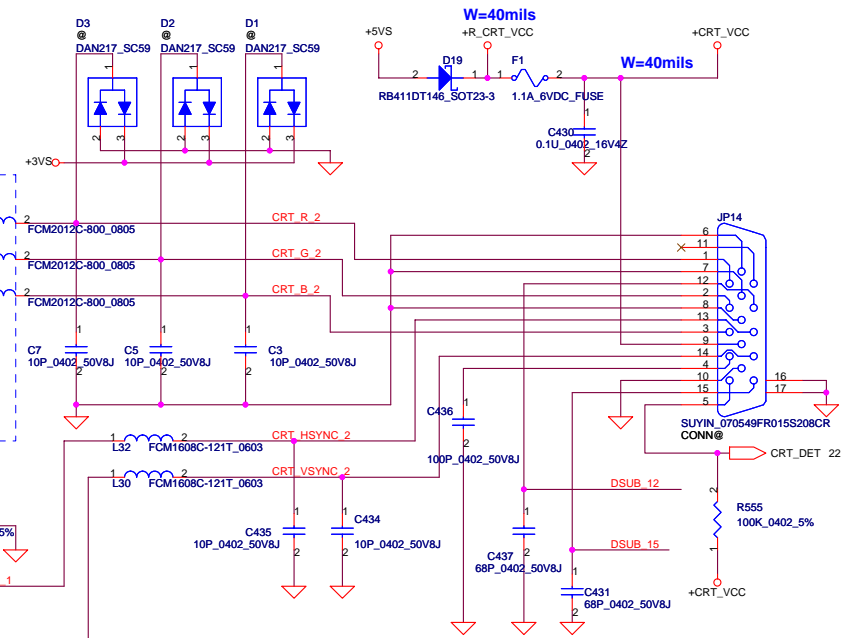
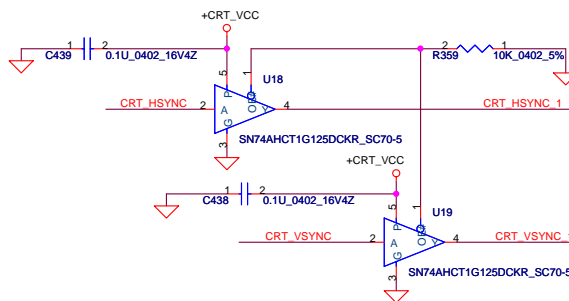
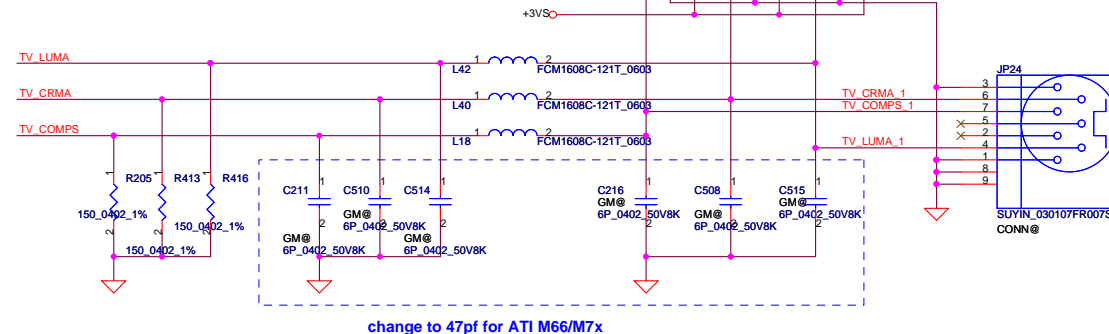
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				Document Number	Rev
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# CRT Connector

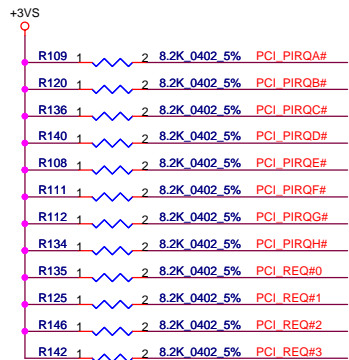
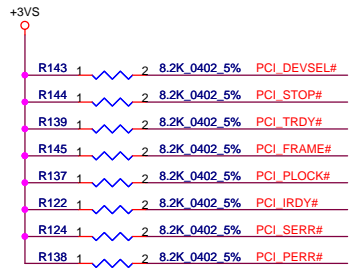


Place closed to chipset

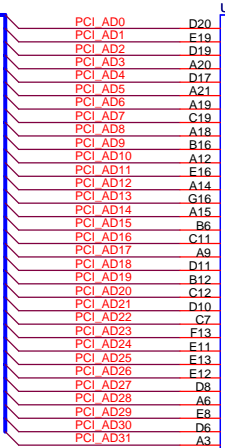
## TV-OUT Conn.



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Issued Date	2006/12/25	Deciphered Date	2007/12/25	CRT & TV-OUT Connector	
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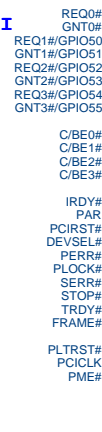


25 PCI\_AD[0..31]

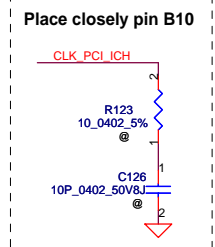
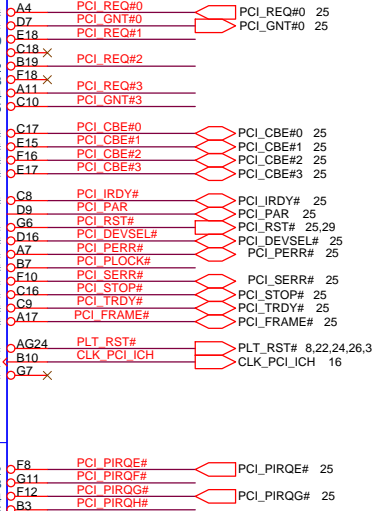
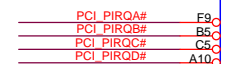


USB

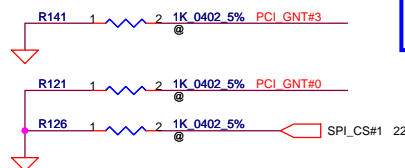
PCI



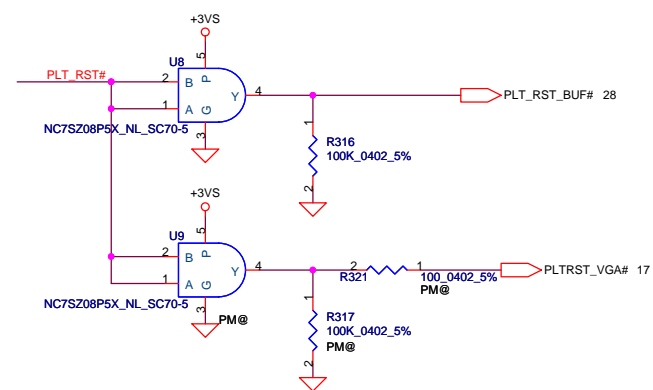
Interrupt I/F

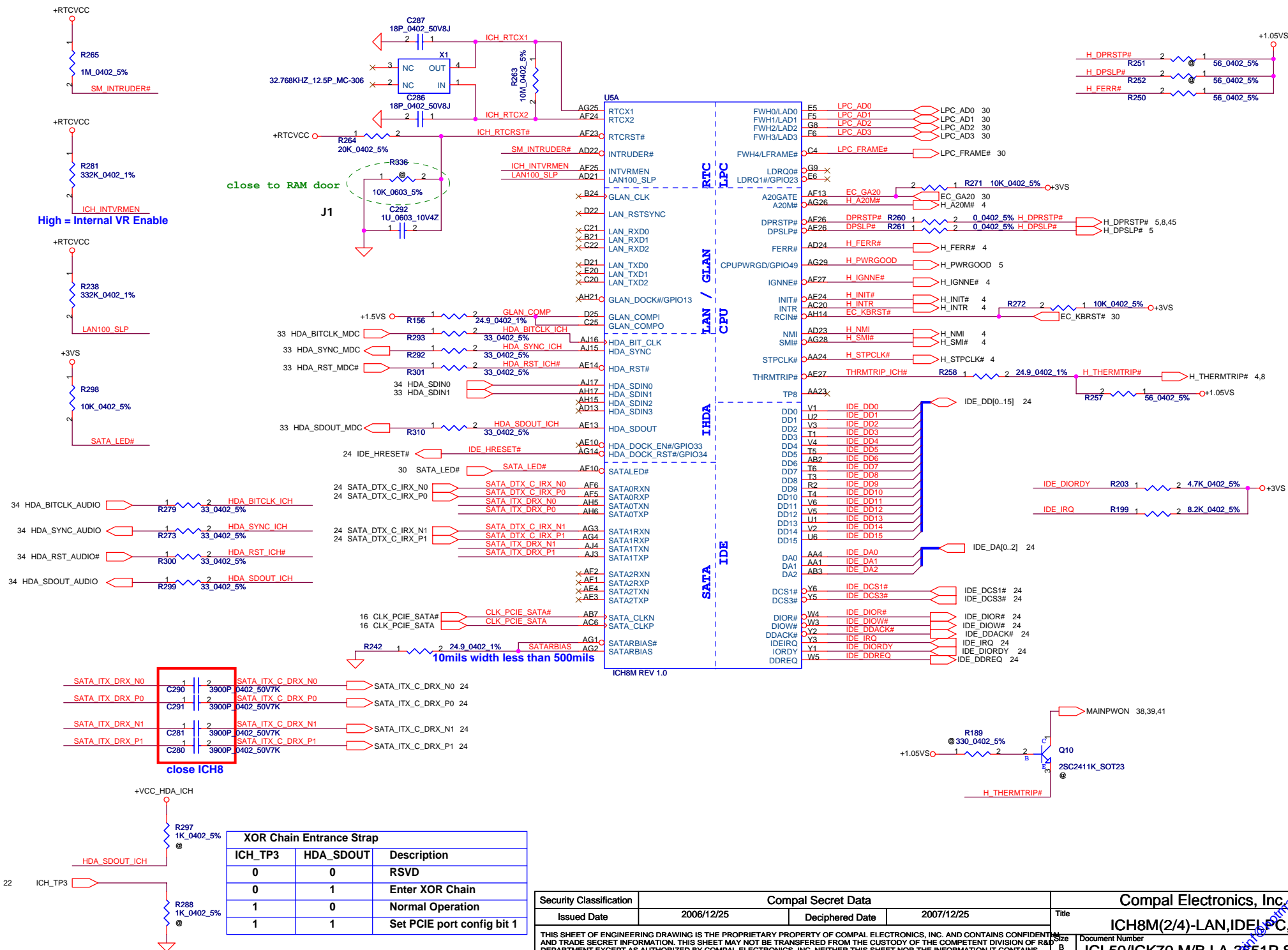


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

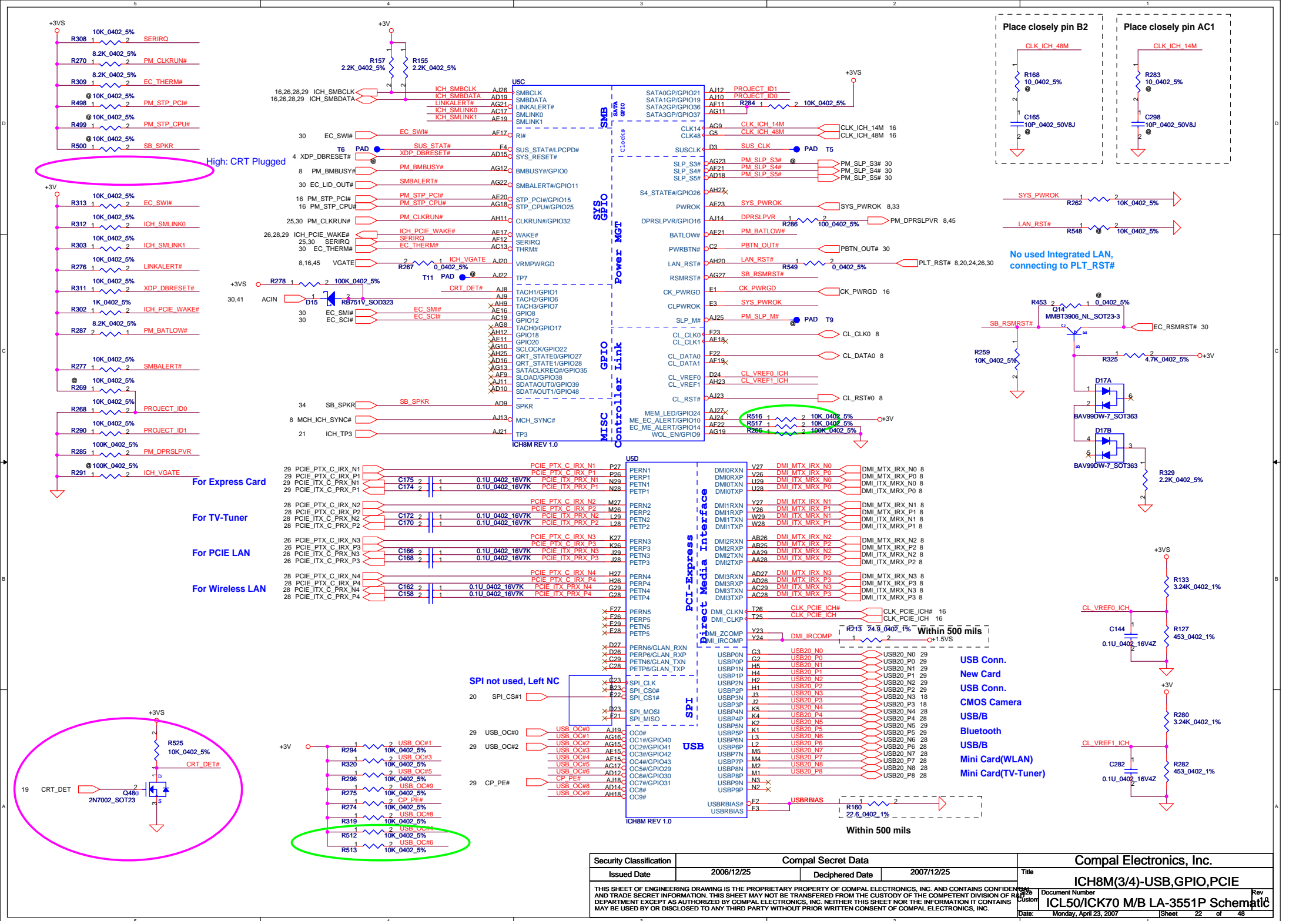


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

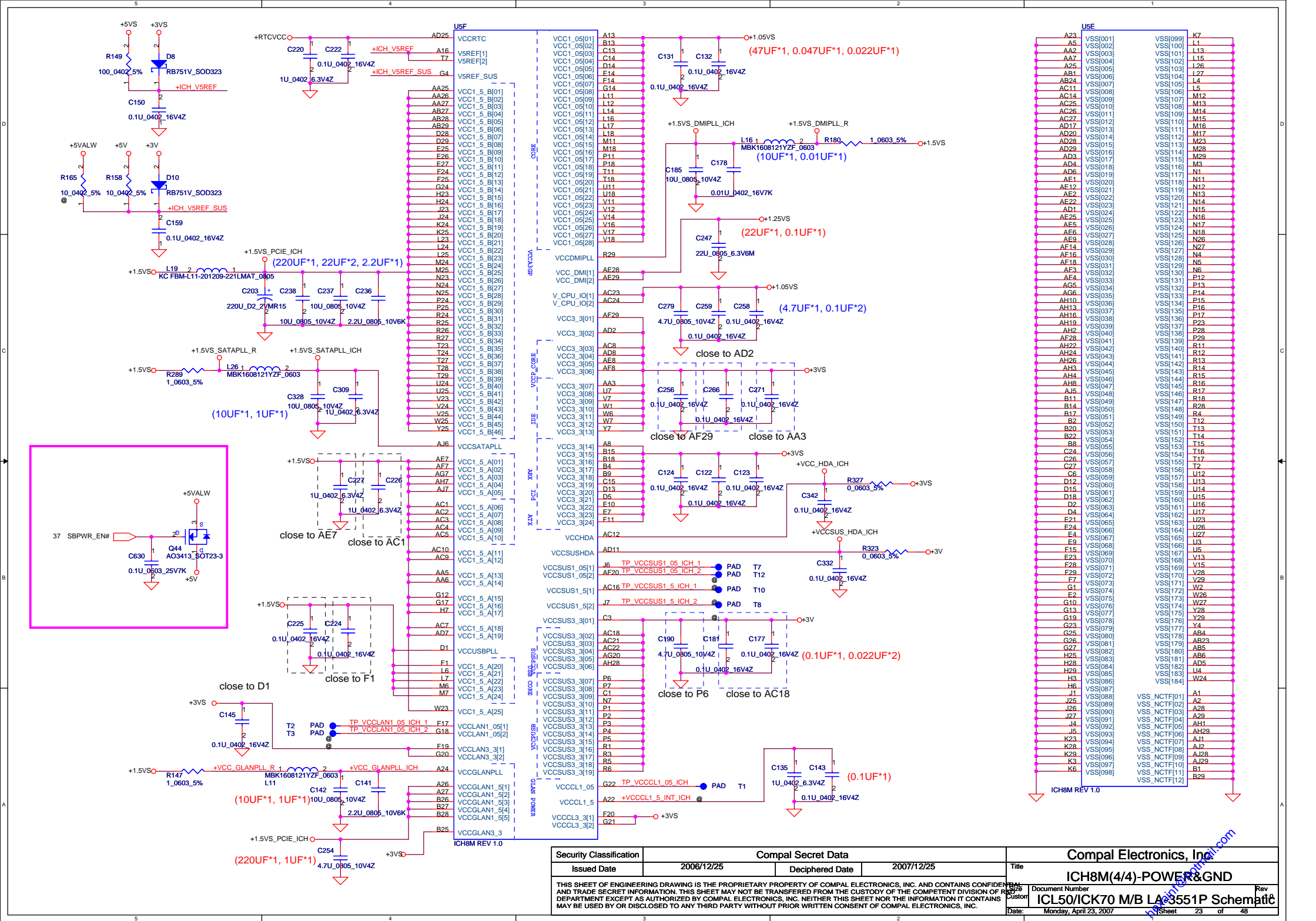


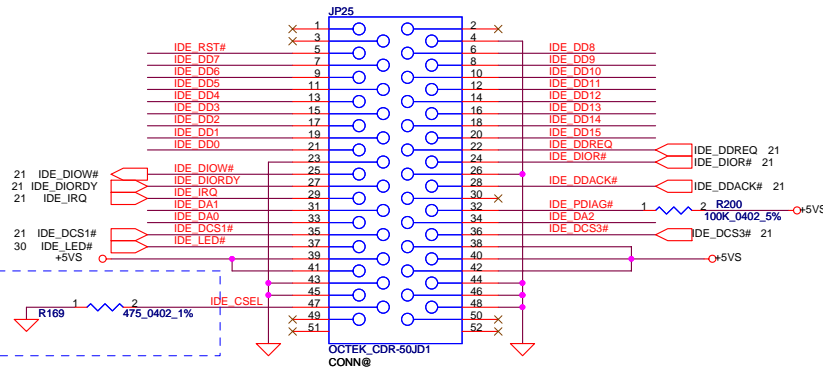




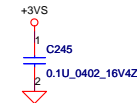
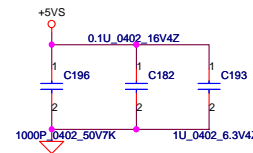








+5VS ○ 2 1 100K\_0402\_5% IDE\_LED#



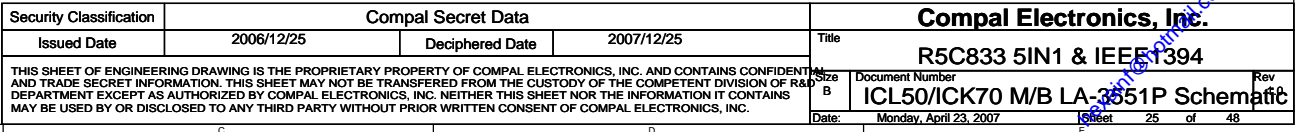
**J27**

Pin	Signal
1	GND
2	HTX0+
3	HTX0-
4	GND
5	HRX0+
6	HRX0-
7	GND
8	VCC3.3
9	VCC3.3
10	VCC3.3
11	GND
12	GND
13	GND
14	VCC5
15	VCC5
16	VCC5
17	GND
18	RESERVED
19	GND
20	VCC12
21	VCC12
22	VCC12
23	GND
24	HTX1+
25	HTX1-
26	GND
27	HRX1+
28	HRX1-
29	GND
30	GND1
31	GND2

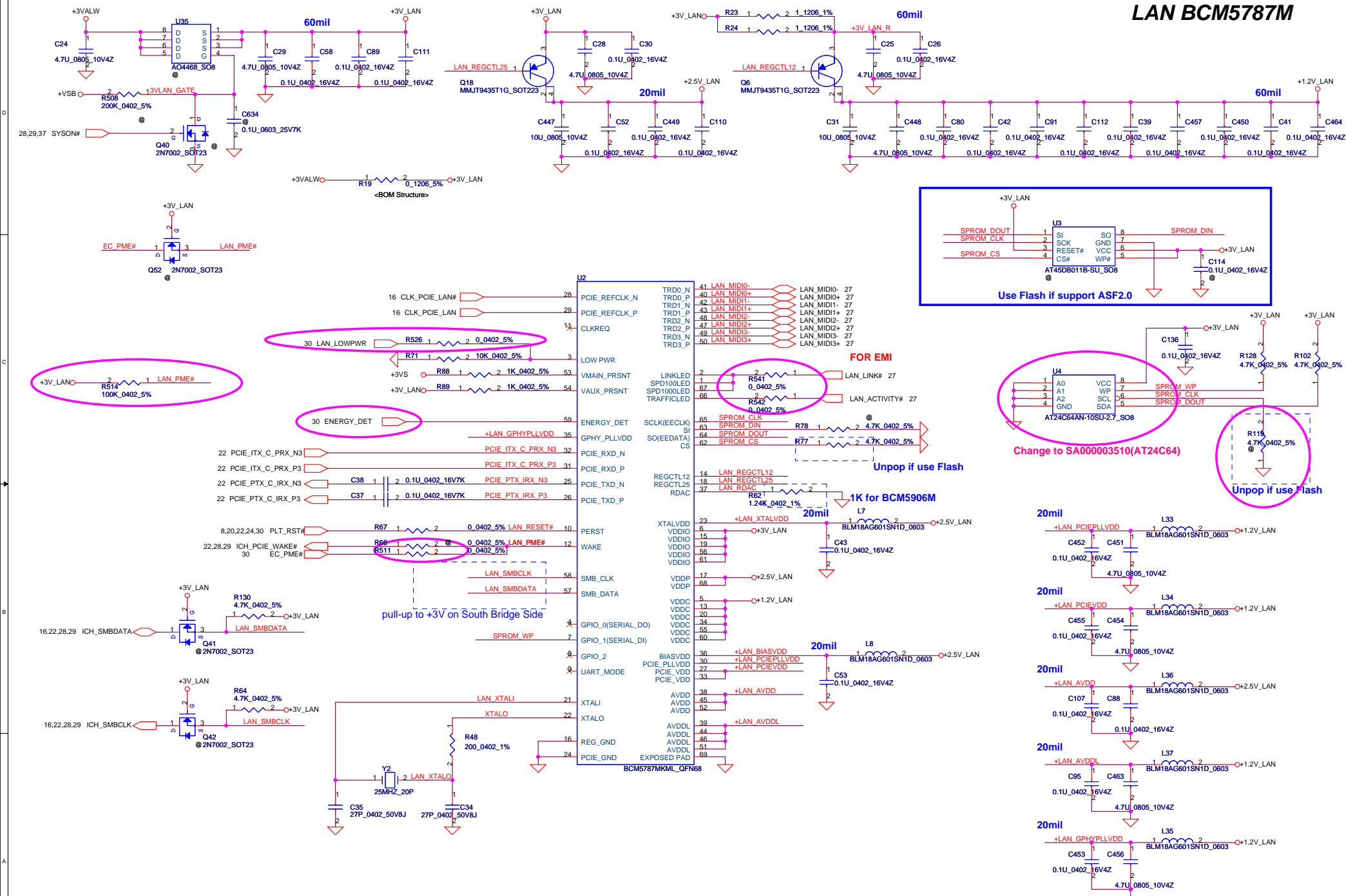
**CTEK SAS-22CA1**  
**CONN@**

2nd HDD for 17"

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				ICL50/CK70 M/B LA-3551P Schematic	1
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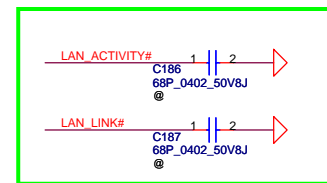


**LAN BCM5787M**



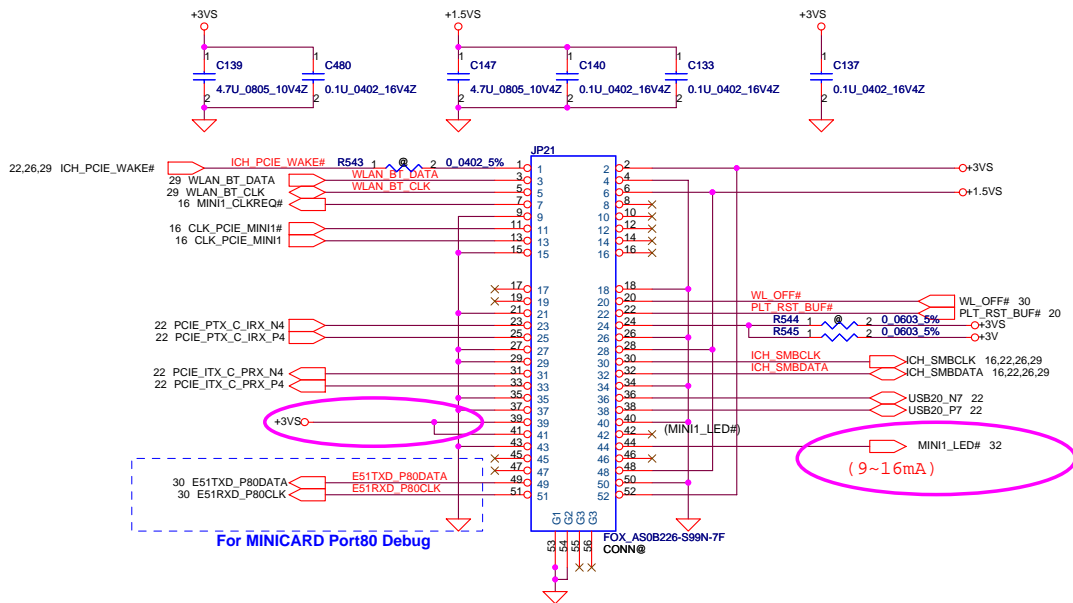
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The schematic diagram illustrates the internal circuitry of a USB-to-Ethernet adapter. At the top, two PSOT24C-LF-T7\_SOT23-3 components (D30 and D31) are shown, connected to the LAN\_LINK# and LAN\_ACTIVITY# signals. The main circuit is powered by +3V\_LAN and +3V\_LAN\_GND. The LAN\_LINK# and LAN\_ACTIVITY# signals are connected to the USB connector (JP18) and the RJ45 connector. The RJ45 connector is connected to the FOX\_JM36113-L2R8-7F CONN@ chip. The circuit includes various capacitors (C94, C151, C154, C186, C187, C108, C96) and resistors (R70, R154). The RJ45 connector is labeled with RJ45\_MIDI3-, RJ45\_MIDI3+, RJ45\_MIDI1-, RJ45\_MIDI1+, RJ45\_MIDI2-, RJ45\_MIDI2+, RJ45\_MIDI0-, and RJ45\_MIDI0+.



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				Size	Document Number	Rev			
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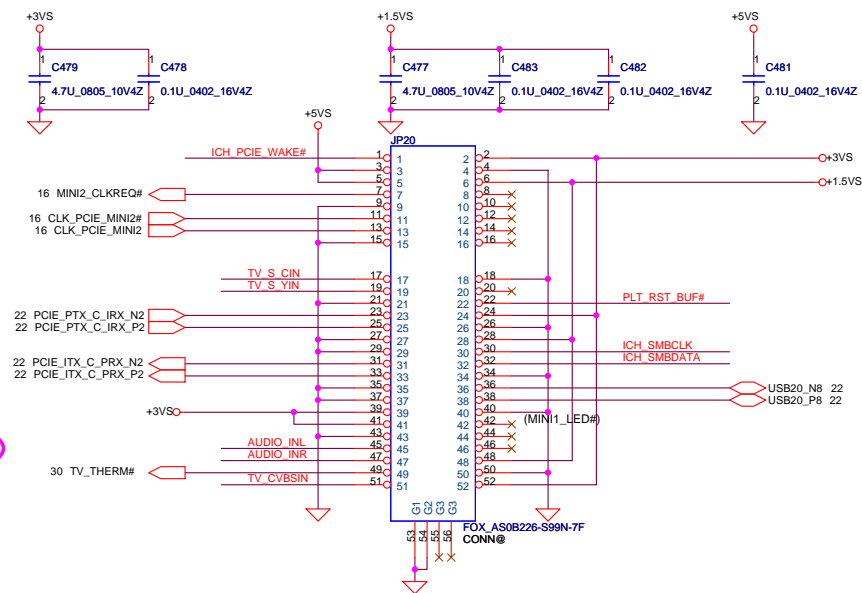
## For Wireless LAN



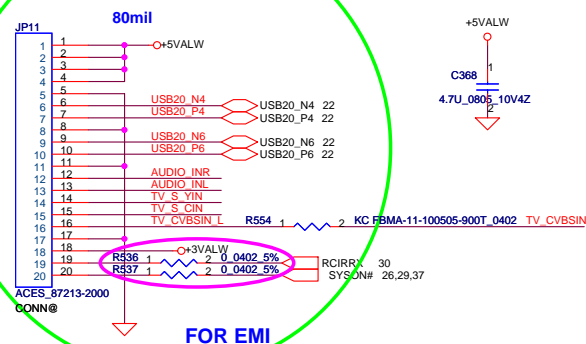
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

## For TV-Tuner/HW MPEG



## To USB/B Connector

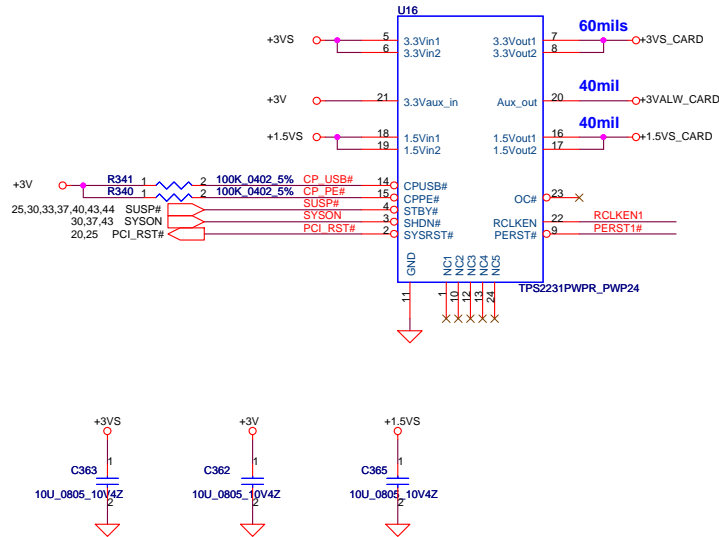


AV-IN Connector  
CIR

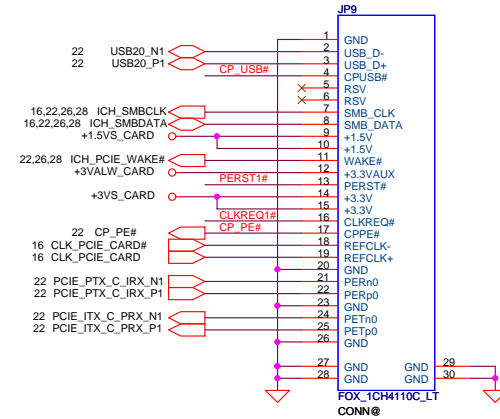
FOR EMI

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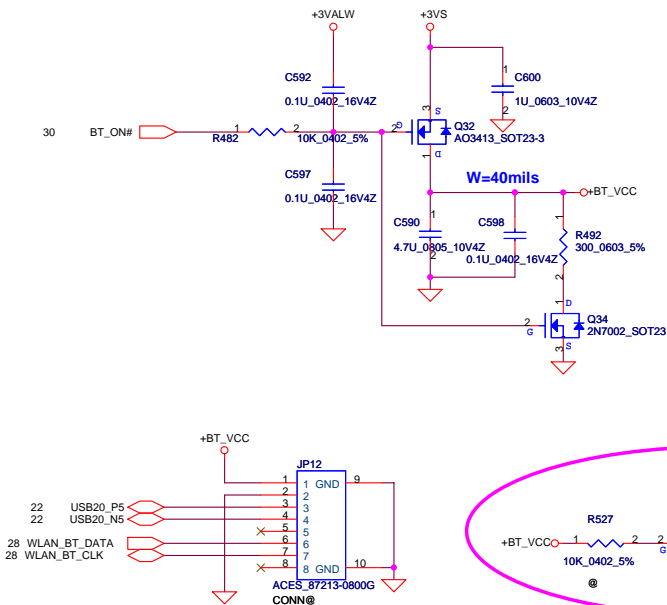
## New Card Power Switch



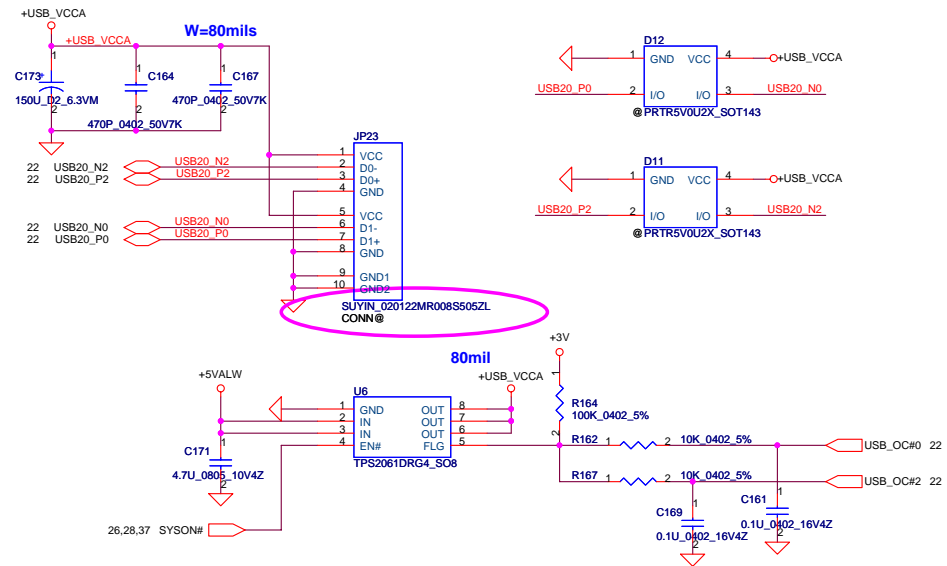
## New Card Socket (Left/TOP)



## Bluetooth Conn.



## USB CONN. (Stack-up Type)



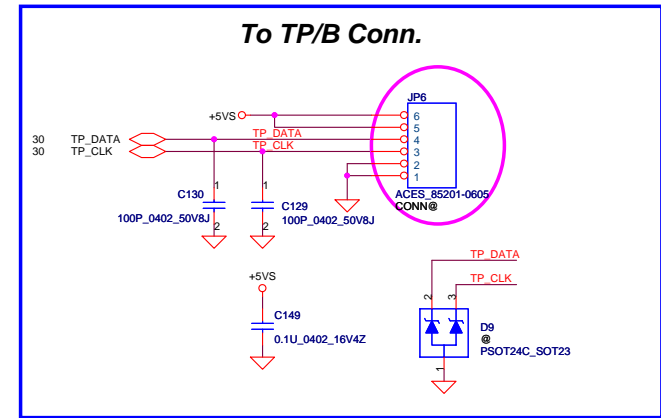
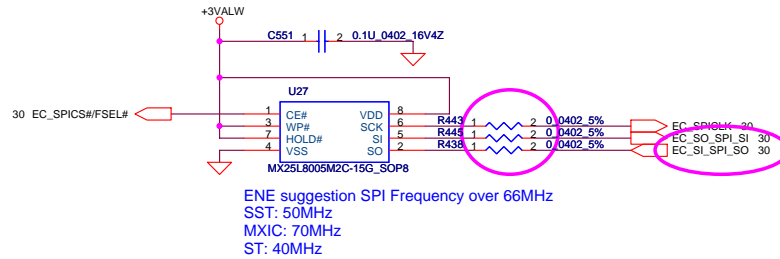
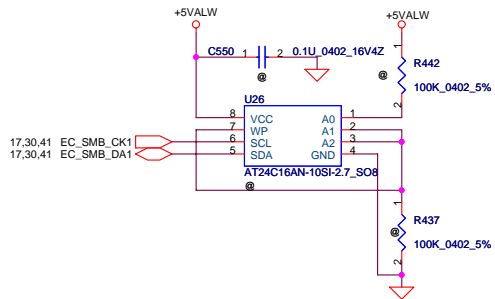
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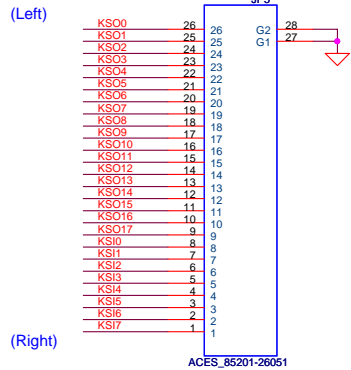


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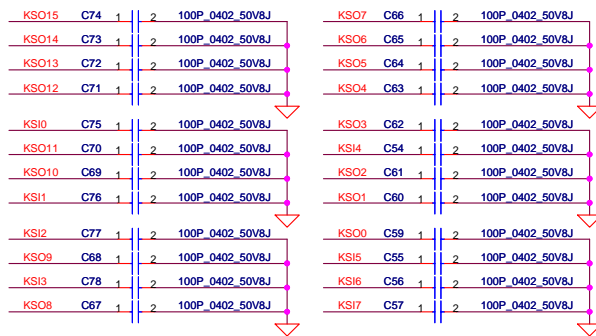


## INT\_KBD Conn.

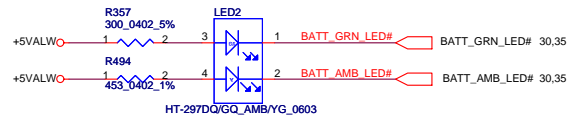
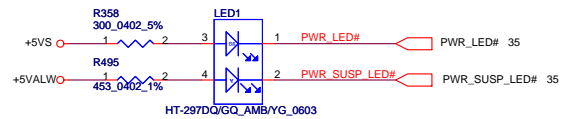
KSII[0..7] 30  
KSO[0..17] 30



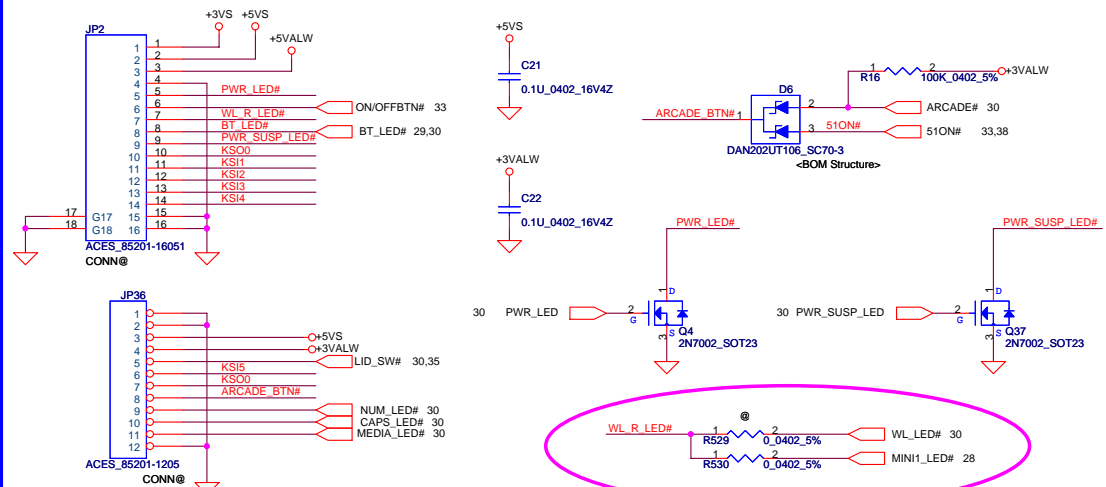
ACES\_85201-26051  
CONN@



## Compal Footprint

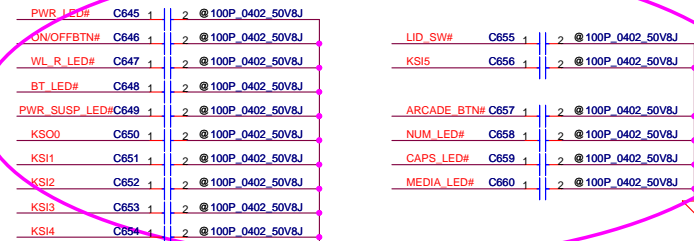


## To BTN/B Conn.



## FOR EMI

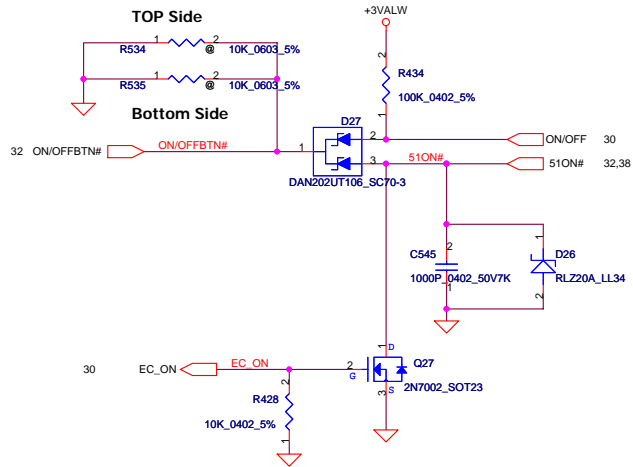
	KSO0
KSII1	WL_BTN#
KSII2	BT_BTN#
KSII3	EMAIL_BTN#
KSII4	IE_BTN#
KSII5	E-KEY_BTN#



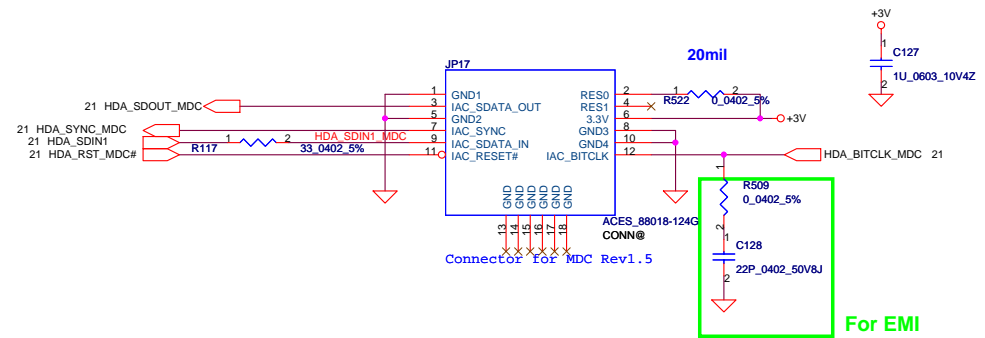
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## Power Button

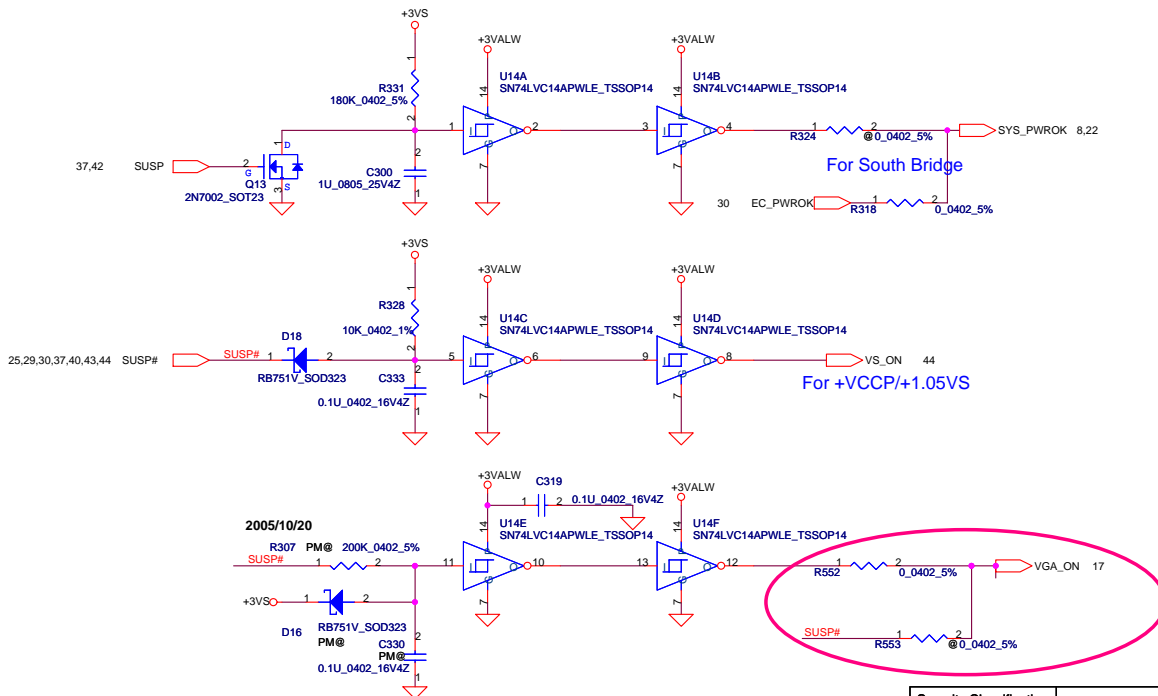
ON/OFF switch



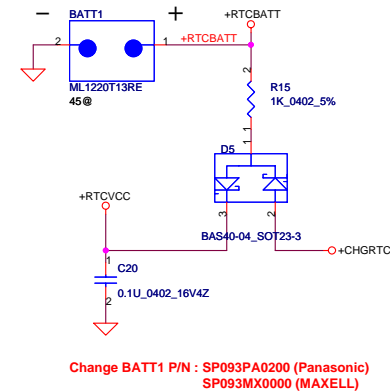
## HDA MDC Conn.



## Power ON Circuit



## RTC Battery

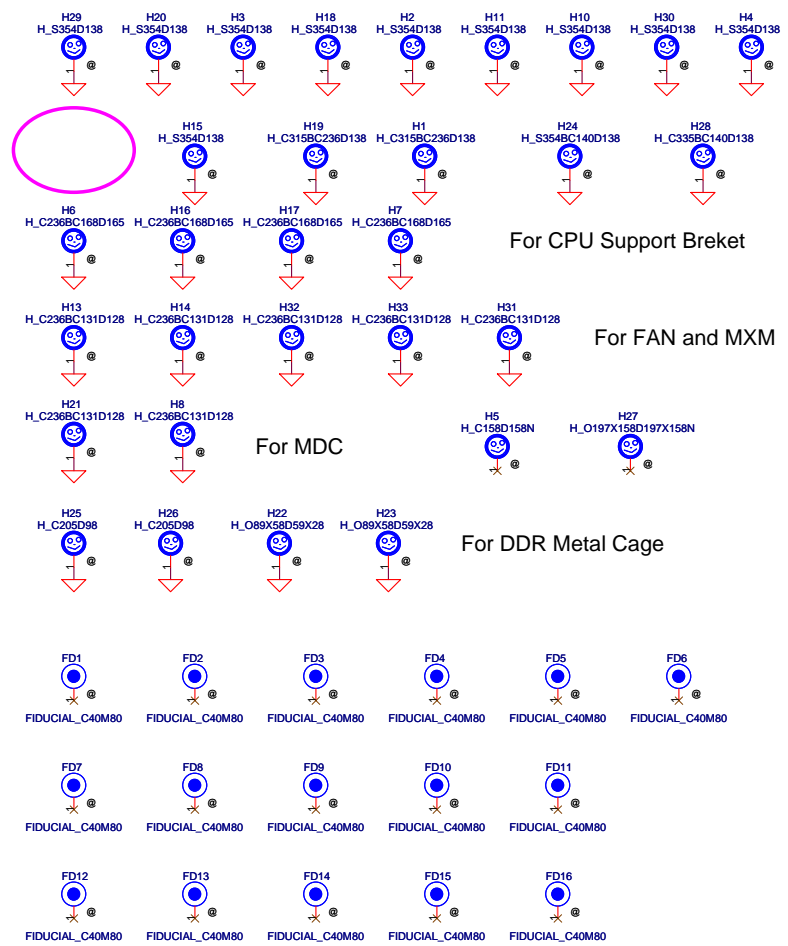
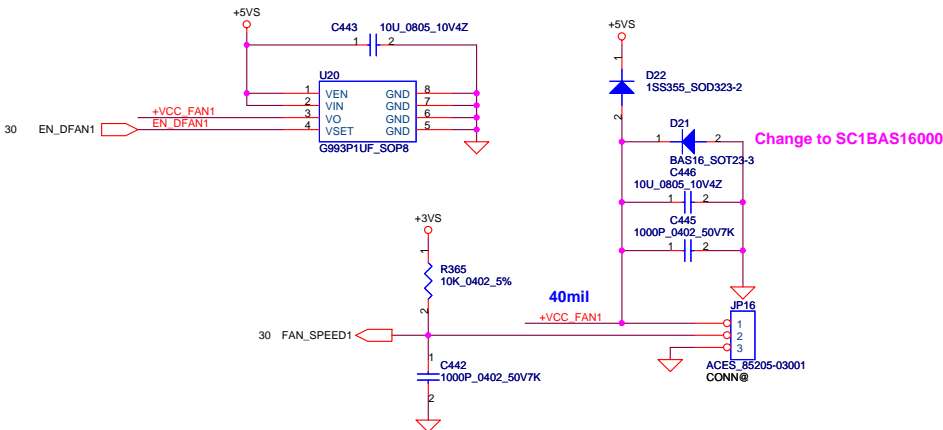


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Deciphered Date				2007/12/25				Power OK, Reset and RTC Circuit, TP			
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				ICL50/ICK70 M/B LA-3551P				Schematic			
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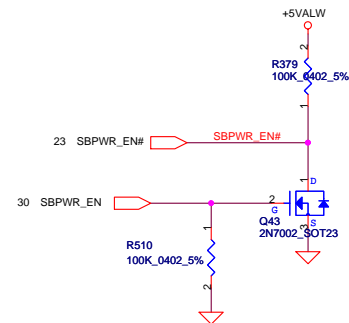
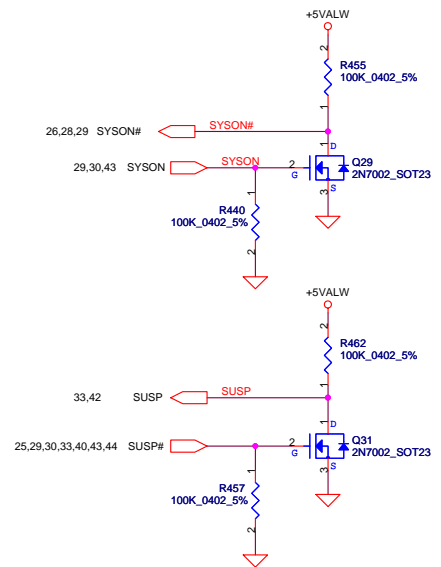
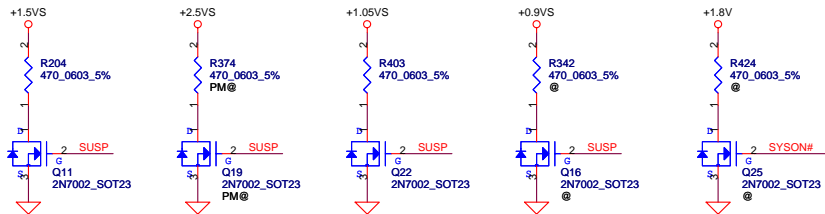
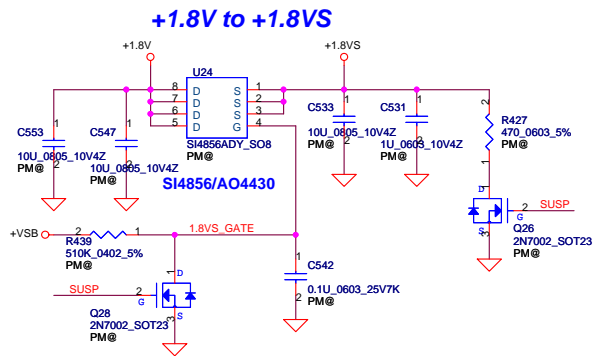
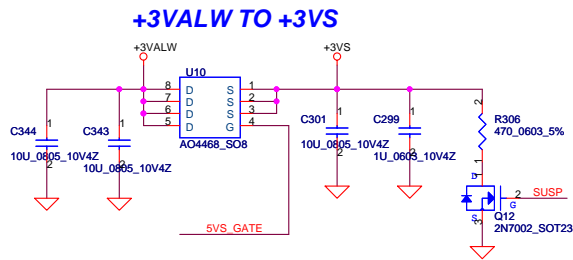
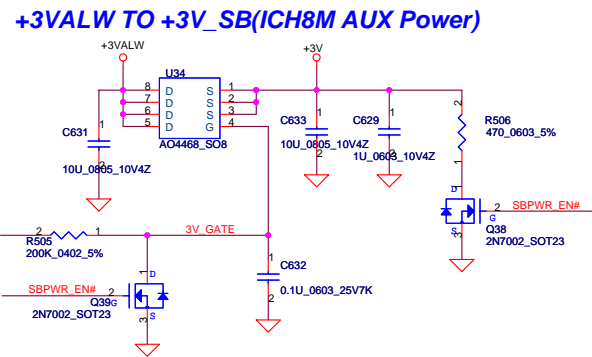
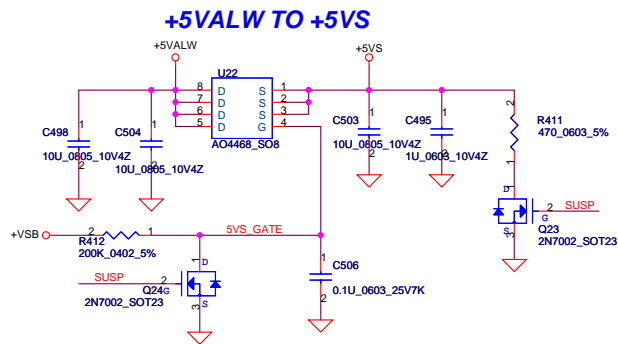


FAN1 Conn

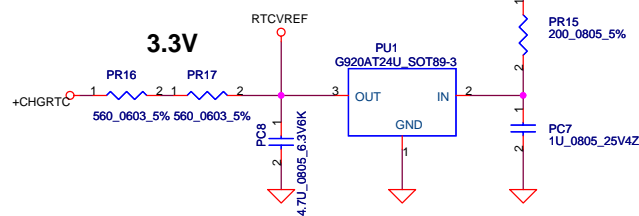
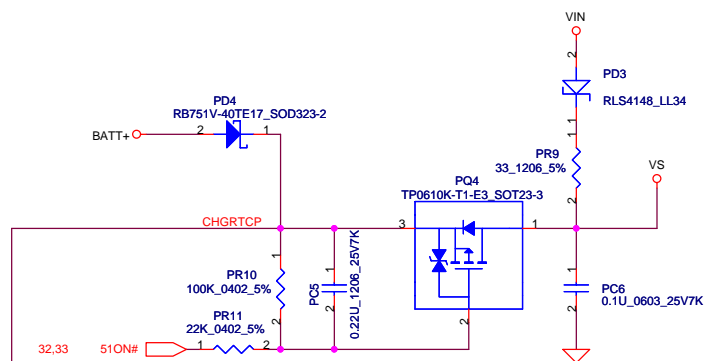
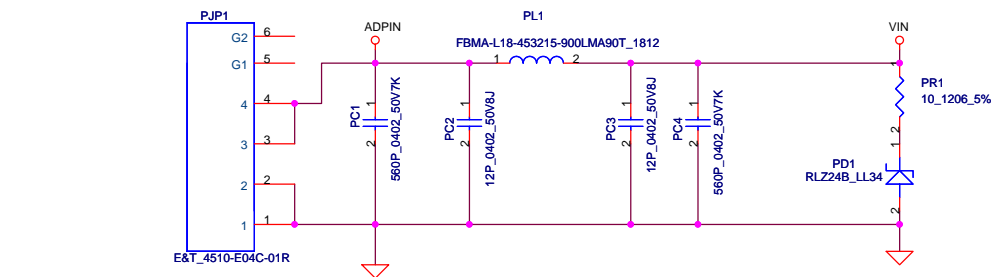


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				ICL50/ICK70 M/B LA-3551P Schematic	1
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				ICL50/ICK70 M/B LA-3551P Schematic	
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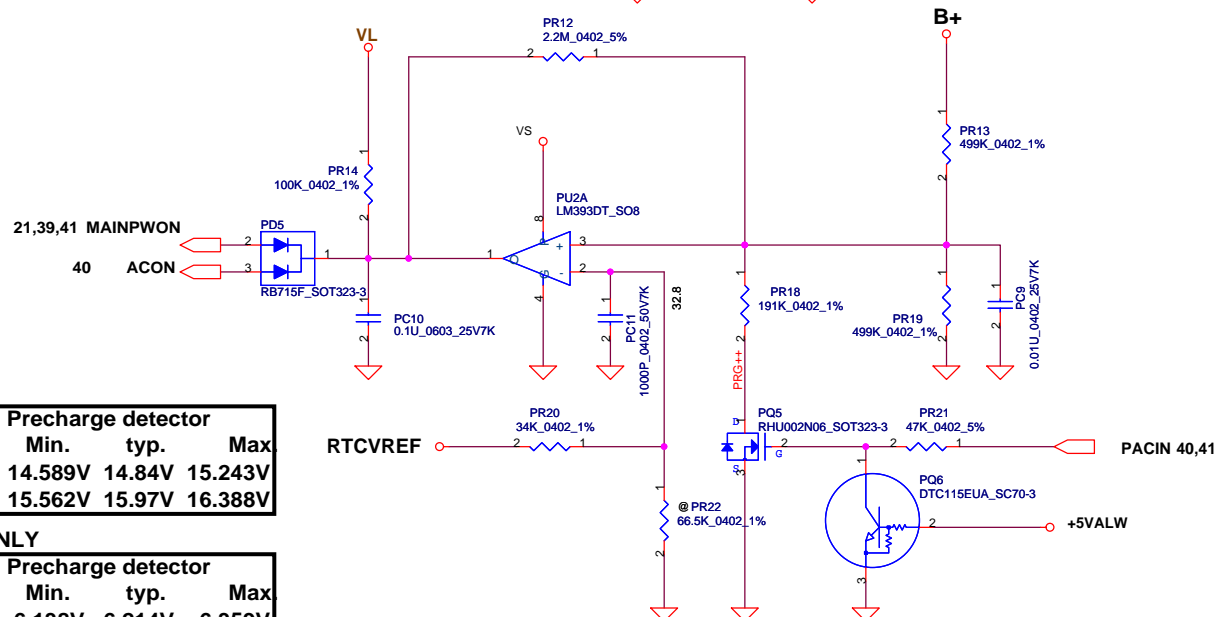
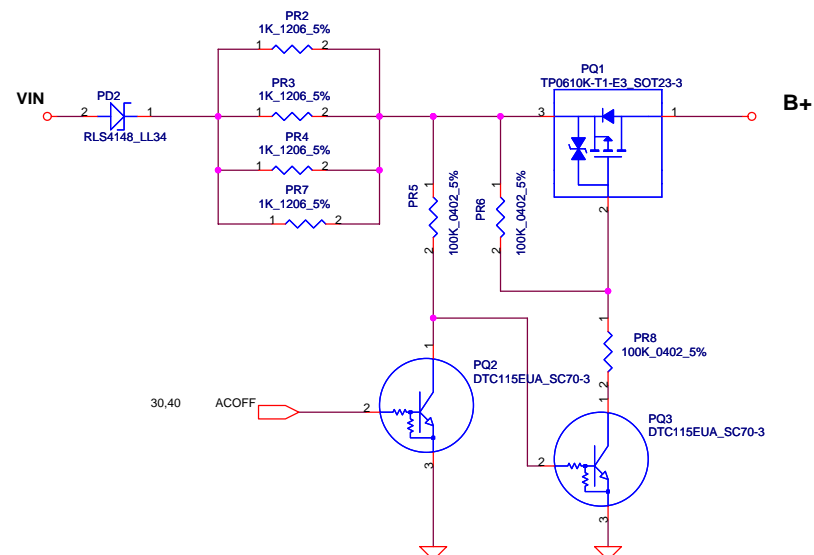


#### ACIN

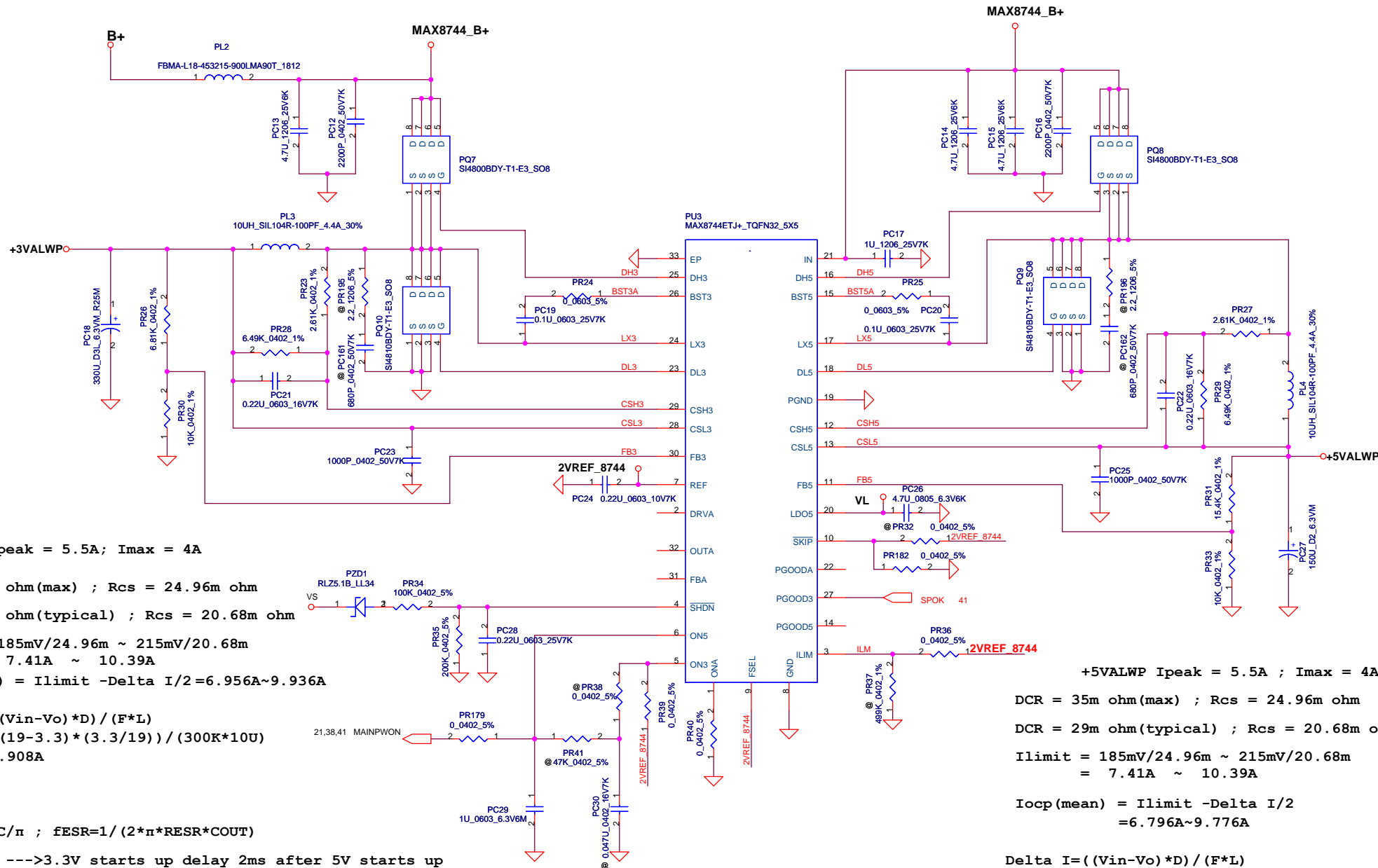
Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

#### BATT ONLY

Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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**+3VALWP Ipeak = 5.5A; Imax = 4A**  
**DCR = 35m ohm(max) ; Rcs = 24.96m ohm**  
**DCR = 29m ohm(typical) ; Rcs = 20.68m ohm**  
**Ilimit = 185mV/24.96m ~ 215mV/20.68m**  
**= 7.41A ~ 10.39A**  
**Iocp(mean) = Ilimit -Delta I/2=6.956A~9.936A**

**Delta I=((Vin-Vo)\*D)/(F\*L)**  
**=((19-3.3)\*(3.3/19))/(300K\*10U)**  
**=0.908A**

**Notes :**  
**fESR<=fOSC/n ; fESR=1/(2\*n\*RESR\*COU)**  
**ON3 = REF --->3.3V starts up delay 2ms after 5V starts up**

**+5VALWP Ipeak = 5.5A ; Imax = 4A**  
**DCR = 35m ohm(max) ; Rcs = 24.96m ohm**  
**DCR = 29m ohm(typical) ; Rcs = 20.68m ohm**  
**Ilimit = 185mV/24.96m ~ 215mV/20.68m**  
**= 7.41A ~ 10.39A**  
**Iocp(mean) = Ilimit -Delta I/2**  
**=6.796A~9.776A**

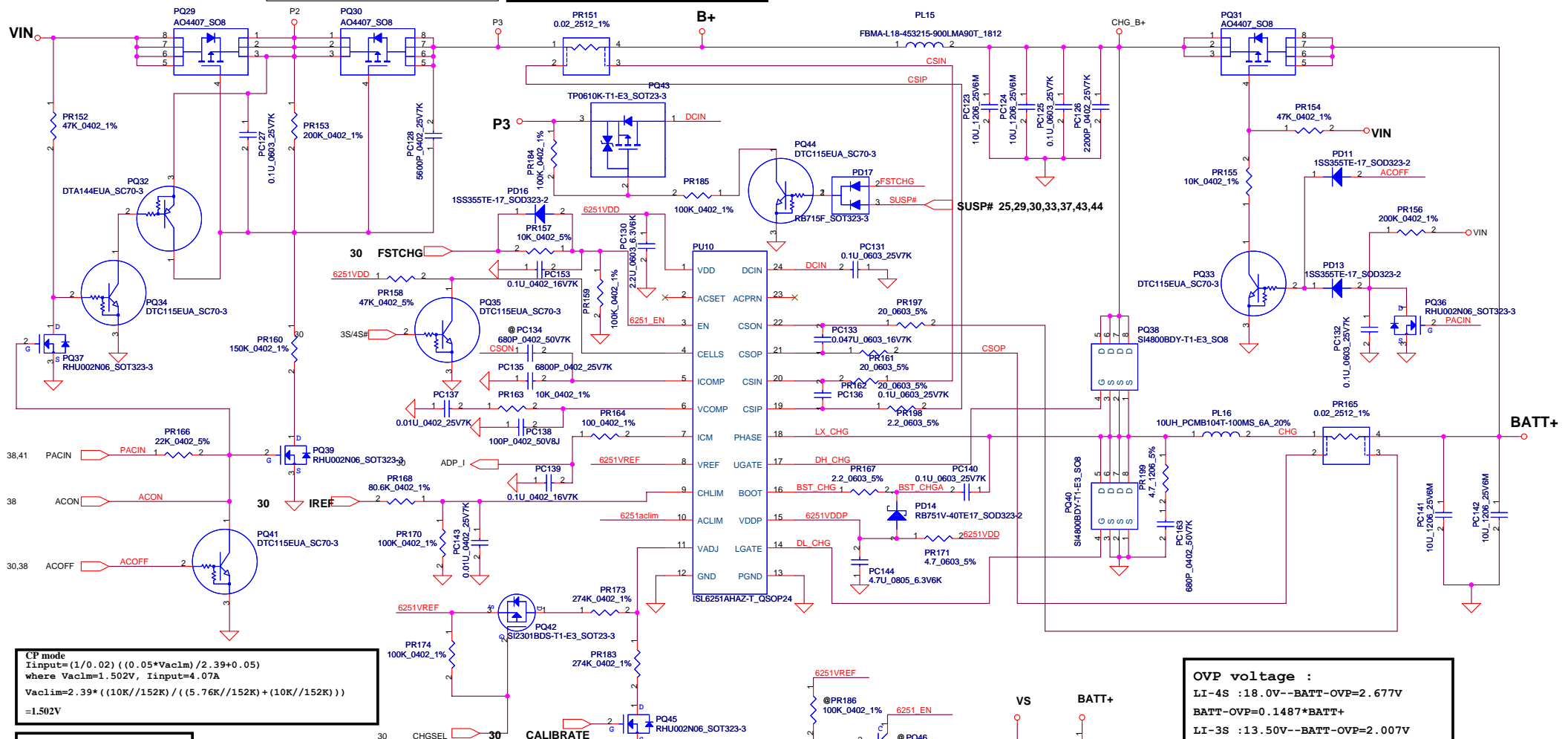
**Delta I=((Vin-Vo)\*D)/(F\*L)**  
**=((19-5)\*(5/19))/(300K\*10U)**  
**1.228A**

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Iada=0~4.74A (90W)

$$ADP\_I = 19.9 * I_{\text{adapter}} * R_{\text{sense}}$$

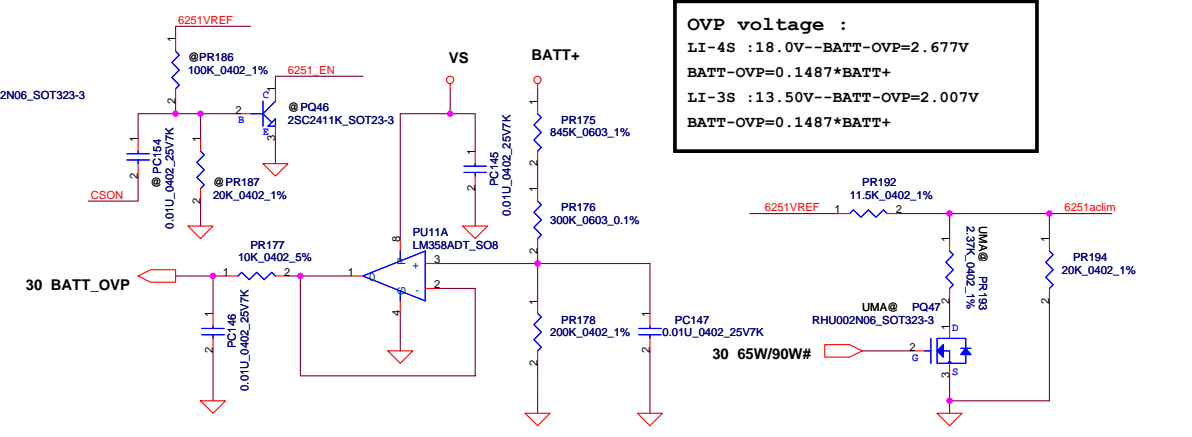
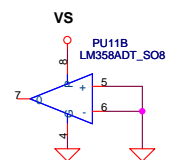
$$CP = 85\% * I_{\text{ada}} ; CP = 4.07A$$



CP mode  
 $I_{\text{input}} = (1/0.02) * ((0.05 * V_{\text{aclim}}) / (2.39 + 0.05))$   
 where  $V_{\text{aclim}} = 1.502V$ ,  $I_{\text{input}} = 4.07A$   
 $V_{\text{aclim}} = 2.39 * ((10K // 152K) / ((5.76K // 152K) + (10K // 152K)))$   
 $= 1.502V$

CC=0.6~4.48A  
 $I_{\text{REF}} = 0.7224 * I_{\text{charge}}$   
 $I_{\text{REF}} = 0.43V \sim 3.24V$

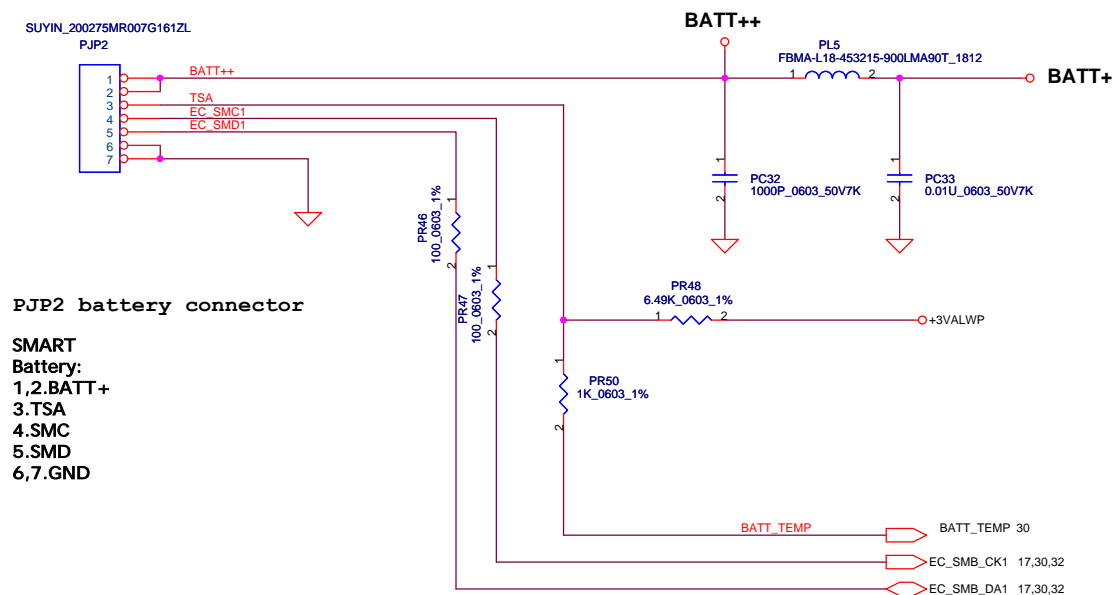
BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V



OVP voltage :  
 LI-4S : 18.0V -- BATT-OVP = 2.677V  
 BATT-OVP = 0.1487 \* BATT+  
 LI-3S : 13.50V -- BATT-OVP = 2.007V  
 BATT-OVP = 0.1487 \* BATT+

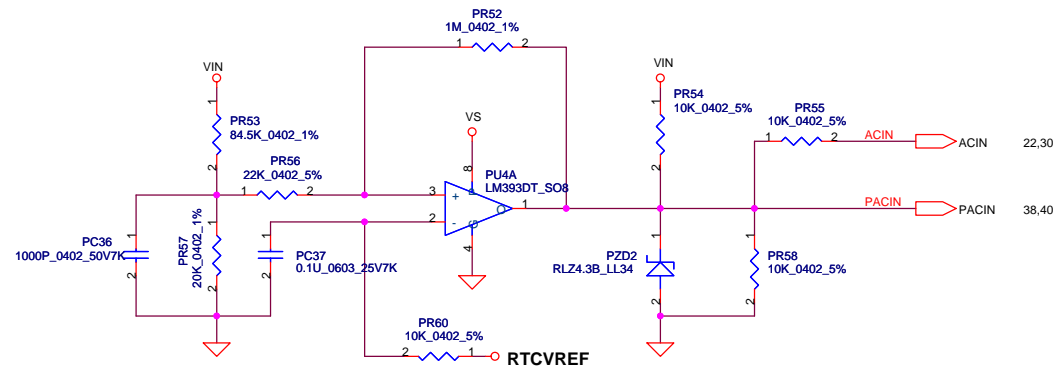
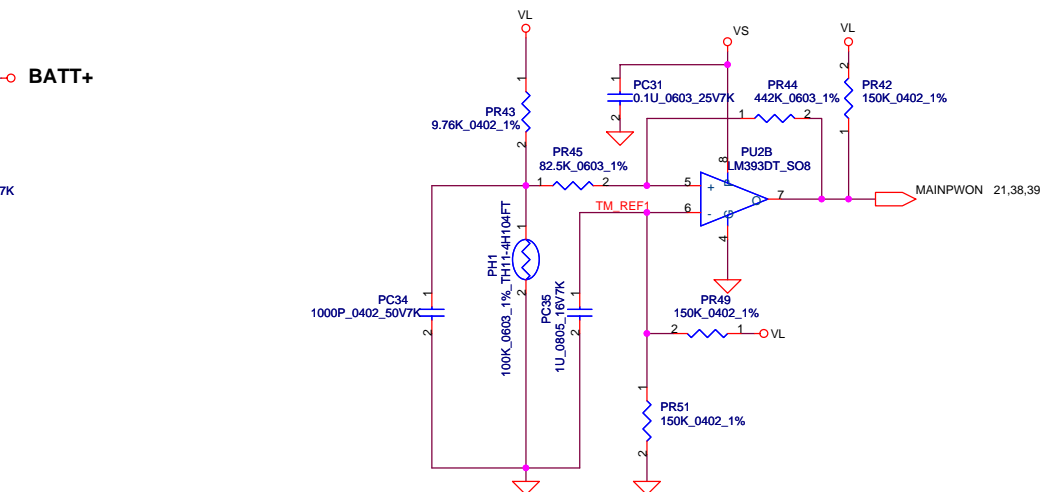
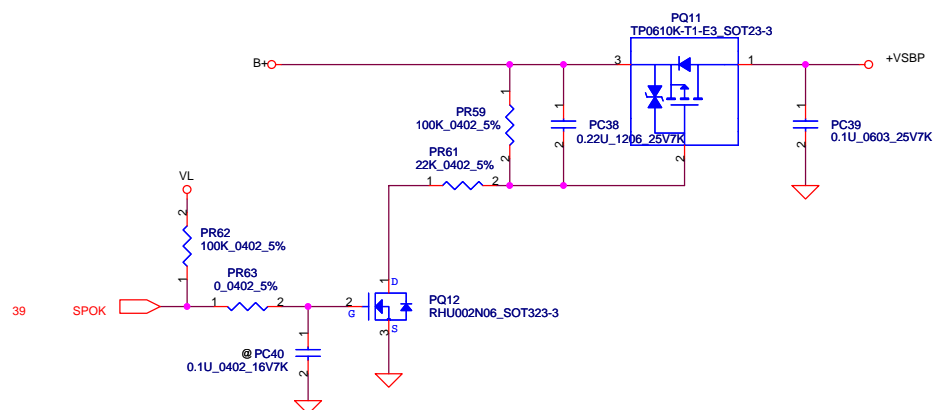
PH1 under CPU botten side :  
CPU thermal protection at 90 degree C  
Recovery at 70 degree C

SUYIN\_200275MR007G161ZL  
PJP2



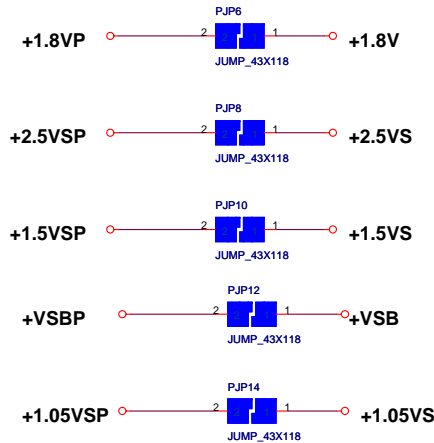
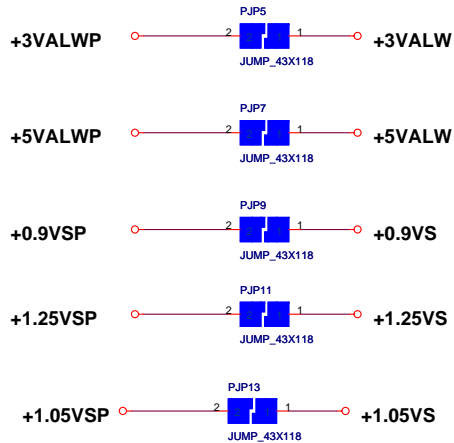
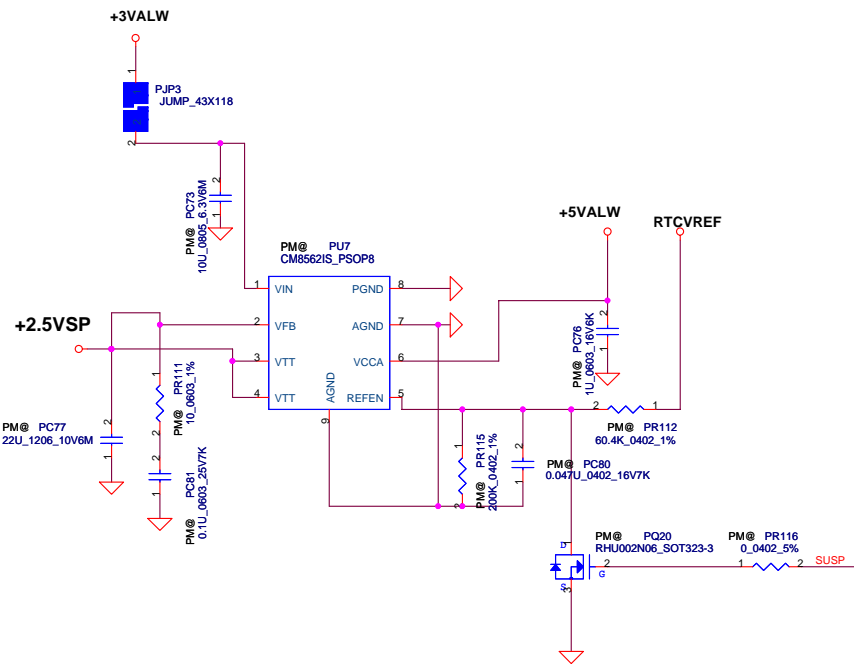
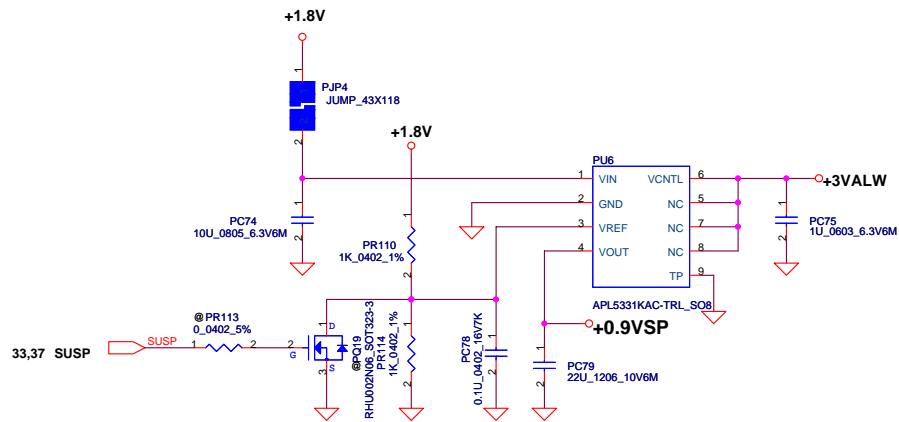
PJP2 battery connector

SMART  
Battery:  
1,2.BATT+  
3.TSA  
4.SMC  
5.SMD  
6,7.GND



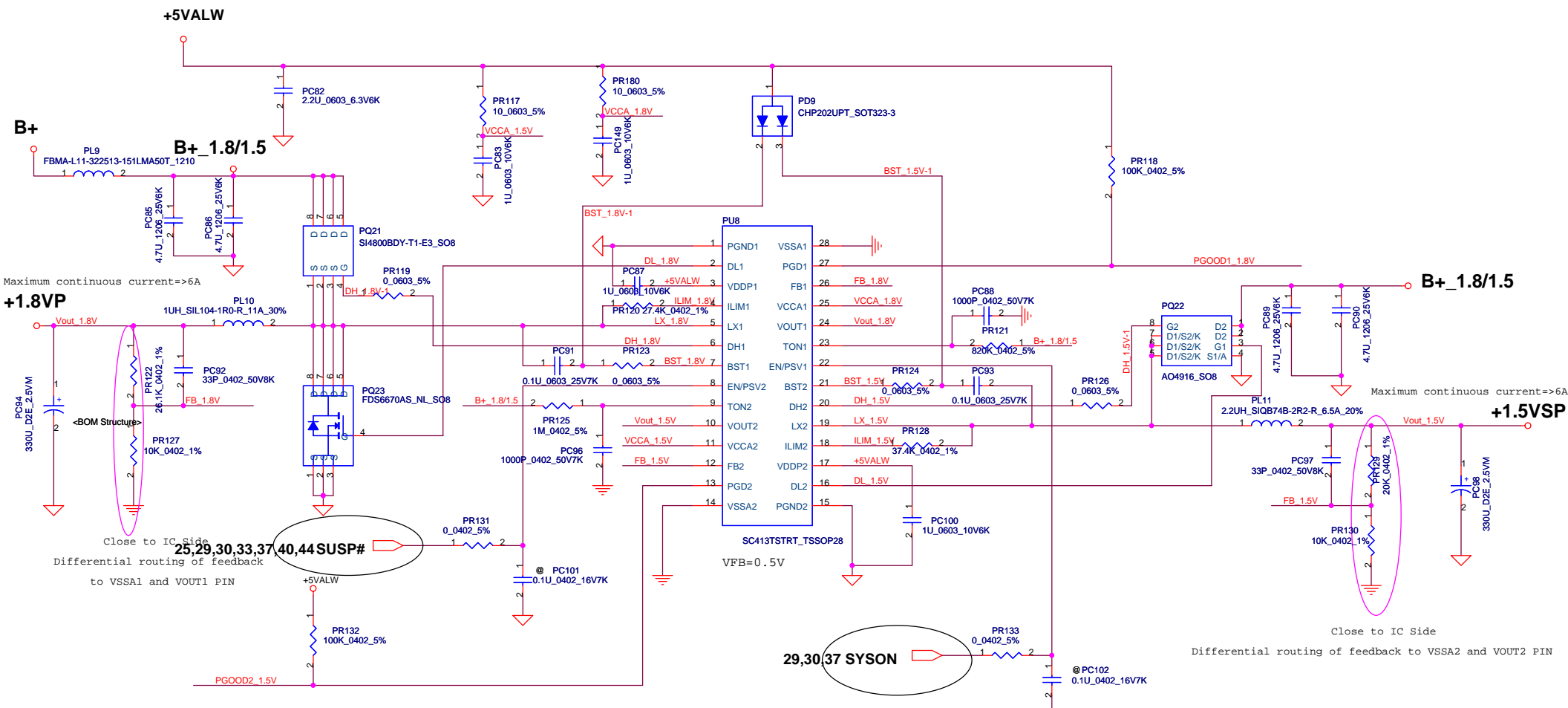
Vin Detector		
Min.	typ.	Max.
H-->L 16.976V	17.257V	17.728V
L-->H 17.430V	17.901V	18.384V

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Title				+0.9VSP/+2.5VSP				Title			
Document Number				ICL50/ICK70				Document Number			
Date				Thursday, April 18, 2007				Date			
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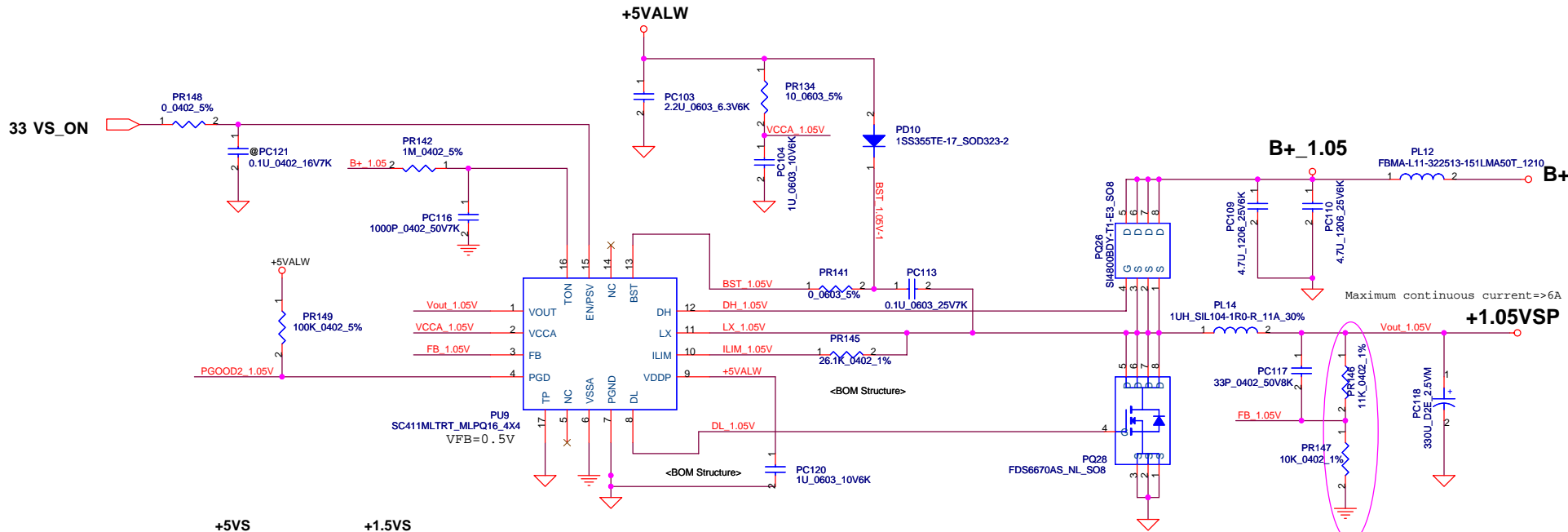




VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
**Ipeak=11.73A, I<sub>max</sub>=8.211A**  
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$   
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$   
FDS6670AS:Rds(on)=>Typ:9 mOhm  
Max:11.5 mOhm  
 $I_{ocp} = I_{valley} + "I_{ripple} / 2$   
 $I_{ripple} = (vin - vout) * (Ton / L) = 5.467A, 1/2 I_{ripple} = 2.734A$   
 $I_{valleymin} = 10E-6 * (PR120 / Rds(ON))_{max} * 1.5$   
**= 9\*10e-6 \* (27.4K / 0.0115\*1.5) = 14.295A > 11.73\*1.2 = 14.076A**  
 $I_{valleymax} = 10E-6 * (PR120 / Rds(ON))_{typ} * 1.2$   
 $= 11*10e-6 * (27.4K / 0.009*1.2) = 27.907A$   
**OCP=>17.029A~30.641A**

VFB=0.5V  
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$   
**Ipeak=4.39A+2.91A=7.3A, I<sub>max</sub>=7.3\*0.7=5.11A**  
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$   
 $= 0.3201us$   
AO4916 Rds(on)=>Typ:21 mOhm  
Max:27 mOhm  
**Ivalleymin=9\*E-6 \* (37.4K / 0.027\*1.4) = 8.904A > 7.3\*1.2 = 8.76A**  
 $I_{valleymax} = 11E-6 * (37.4K / 0.021*1.1) = 17.809A$   
 $I_{ripple} = (vin - vout) * (Ton / L) = 2.546A, 1/2 I_{ripple} = 1.273A$   
 $I_{ocp} = I_{valley} + "I_{ripple} / 2$   
**OCP=>10.177A~19.082A**

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Close to IC Side  
Differential routing of feedback to VSSA2 and VOUT2 PIN

**VFB=0.5V, Ipeak=14.02A, Imax=9.814A**

The current rating of +1.05VSP include +VCC\_GFX current.

$V_o = VFB * (1 + PR146 / PR147) = 1.05V$

$Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.239\mu s$

SI4810BDY:Rds(on) => Typ: 9mOhm  
Max: 11.5 mOhm

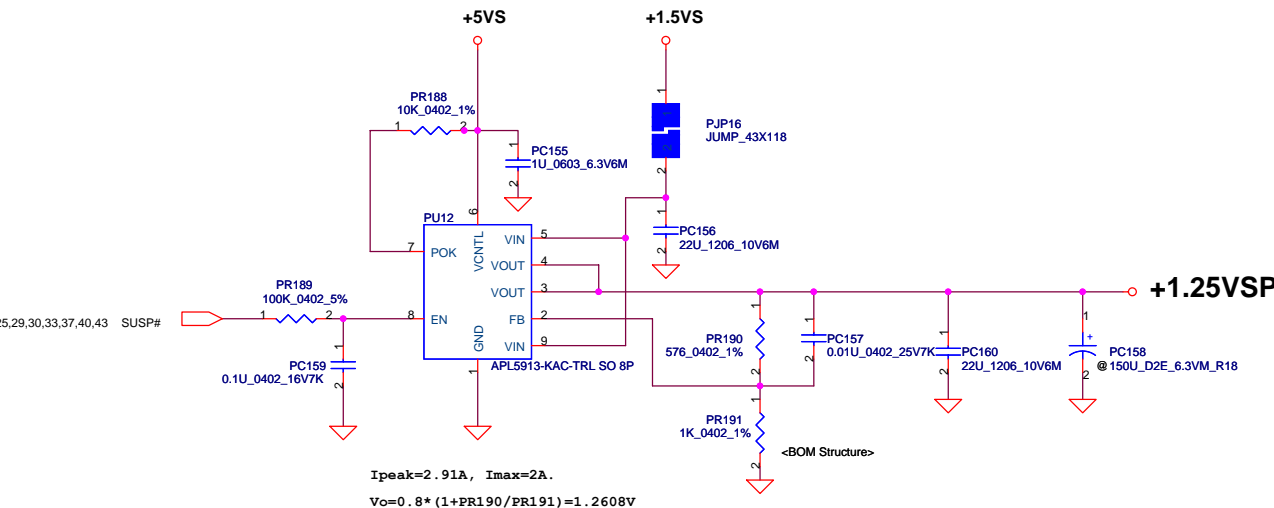
$Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON))max * 1.5$   
 $= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A$

$Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON))min * 1.2$   
 $= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$

$Iripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Iripple = 2.146A$

$Iocp = Ivalley + Iripple / 2$

**OCP ==> 15.763A ~ 22.222A**



**Ipeak=2.91A, Imax=2A.**

$V_o = 0.8 * (1 + PR190 / PR191) = 1.2608V$

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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU_CORE high side MOS desine change	In order to prevent EOL of SI7840, change to SI7686.	0.1	45	Change PQ13 and PQ16 form SB578400080(S TR SI7840DP-T1-E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N SO8).	10/30/06	EVT
2	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ43 SB906100210( S TR TP0610K)	12/21/06	DVT
3	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ44 SB301150000(S TR DTC115EUA)	12/21/06	DVT
4	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD16 SC1SS355010( S DIO 1SS355) Delete PD12 SC1SS355010( S DIO 1SS355)	12/21/06	DVT
5	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD17 SCSB715F000(S DIO RB715F)	12/21/06	DVT
6	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR184,PR185 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
7	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC153 SE076104K80(S CER CAP 0.1U 0402 16V K X7R)	12/21/06	DVT
8	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ45 SB502060000(S TR RHU002N06)	12/21/06	DVT
9	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ46 SB324110010(S TR 2SC411K)	12/21/06	DVT
10	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR183 SD034274380(S RES 1/16W 274K 0402 1%)	12/21/06	DVT
11	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR186 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
12	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR187 SD034200280(S RES 1/16W 20K 0402 1%)	12/21/06	DVT
13	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC154 and PC146 SE075103K80(S CER CAP 0.01U K 25V X7R 0402)	12/21/06	DVT
14	Noise issue in S3 mode and idle mode.	In order to prevent noise issue in S3 mode and idle mode.	0.2	40	Add PC42 SF22004M210(S CAP 220U 25V_M)	12/21/06	DVT
15	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Change PR157 from SD028000080(s res 1/16w 0 0402 5%) TO SD0281000280(S RES 1/16W 10K 0402 5%)	12/21/06	DVT
16	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR34 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100380(S RES 1/16W 100K 0402 5%)	12/21/06	DVT
17	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR35 SD028100380( S RES 1/16W 100K 0402 5%) to SD028200380(S RES 1/16W 200K 0402 5%)	12/21/06	DVT
18	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PC28 from SE042104K80(S CER CAP 0.1U 25V K X7R 0603) to SE000005ZM8(S CER CAP 0.22U 25V K X7R 0603)	12/21/06	DVT
19	CPU MOSFET switching has interference.	Improve CPU switching interference.	0.2	45	Change PC69,PC70,PC71,PC72 from SE082221J80 to SE068102J80 (S CER CAP 1000P 25V J NPO 0402)	12/21/06	DVT
20	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PU7 SA085620080 from X63470BOL01.	12/21/06	DVT
21	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PQ20 SB502060000 from X63470BOL01.	12/21/06	DVT
22	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR111 SD014100A80 from X63470BOL01.	12/21/06	DVT
23	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR112 SD034604280 from X63470BOL01.	12/21/06	DVT

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1	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR115 SD034200380 from X63470BOL01.	10/30/06	EVT
2	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR116 SD028000080 from X63470BOL01.	12/21/06	DVT
3	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC73 SE142475K80 from X63470BOL01.	12/21/06	DVT
4	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC76 SE135105K80 from X63470BOL01.	12/21/06	DVT
5	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC77 SE116226M80 from X63470BOL01.	12/21/06	DVT
6	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC80 SE076473K80 from X63470BOL01.	12/21/06	DVT
7	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC81 SE042104K80 from X63470BOL01.	12/21/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ25 SB548000310 (S TR SI4800BDY).	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ27 SB548100020 (S TR 4810BDY)	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PD10 from SC1P202U010 to SC1SS355010.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR135 SD034100380.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR140,SD013000080, PR150 SD028000080.	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR181 SD013100A80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR139 SD034150280.	12/27/06	DVT
15	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR144 SD034100280	12/27/06	DVT
16	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR137 SD034105280.	12/27/06	DVT
17	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR138 SD028100480.	12/27/06	DVT
18	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC105,PC106 SE142475K80.	12/27/06	DVT
19	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC107,PC151 SE080105K80.	12/27/06	DVT
20	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC108 SE074102K80.	12/27/06	DVT
21	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC111 SE042104K80.	12/27/06	DVT
22	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC112 SE068330K80	12/27/06	DVT
24	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PL13 SH000008Y80.	12/27/06	DVT

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1	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC114 SGA20221D30	12/27/06	DVT
2	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PU9 from SA00001FD80 to SA00001FB80	12/27/06	DVT
3	For SMT BOM convenient.	For SMT BOM convenient.	0.3	40	Change PD14 from SC1H751H010 to SC1B751V010.	12/27/06	DVT
4	Increase _1.5VSP OCP point	Increase _1.5VSP OCP point for +1.25VSP new solution.'	0.3	43	Change PR128 from SD034154280 to SD034374380.	12/27/06	DVT
5	Decrease +1.05VSP OCP point.	Decrease +1.05VSP OCP point.	0.3	44	Change PR145 from SD034324280 to SD034261280		DVT
6	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PU12 SA000015410.	12/27/06	DVT
7	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR188 SD034100280.	12/27/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR189 SD034100380.	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR191 SD034100180.	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR190 SD034576080.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC155 SE107105M80.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC156, PC160 SE116226M80	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC157 SE075103K80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC159 SE076104K80.	12/27/06	DVT
15	Increase +1.5VSP output capacitor.	Increase +1.5VSP output capacitor.	0.3	43	Change PC98 from SGA20221D30 to SGA19331D00	12/27/06	DVT
16	Cost issue.	Cost issue.	0.3	44	Change PC118 from SGA20471D00 to SGA19331D00.	12/30/06	DVT
17	BOM issue.	BOM issue.	0.3	45	Change PH3, PH4 from SL210021F20 to SL200000200	12/30/06	DVT
18	Assembly issue.	Due to assembly hard, delete PC42.	0.3	45	Delete PC42 SM22004M210.	12/30/06	DVT
19	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE142475K80 to SE093106M80	01/04/06	DVT
20	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE153106K80 to SE093106M80	01/04/06	DVT
21	Add pull high resister for VAGTE.	Add pull high resister for VAGTE.	0.4	45	Add PR89 SD034200180(S RES 1/16W 2K 0402 1%)	01/04/06	DVT
22	Delete PQ46	PQ46 has potential risk to cause system battery OVP.	0.4	40	Delete PQ46 SB324110010(S TR 2SC411K)	01/04/06	DVT
23	Material shipping issue.	Material shipping issue.	0.4	45	Change PC69, PC70, PC71, PC72 from SE068102J80 to SE074102K80	01/04/06	DVT

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1	Cost down	Cost down	0.5	40	Change PQ38 from SB548100020 to SB548000310.	03/09/07	PVT
2	Cost down	Cost down	0.5	40	Change PQ40 from SB548100020 to SB548000310.	03/09/07	PVT
3	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PR199 SD001470B80 (S RES 1/4W 4.7 1206 +-5%)	04/01/07	Pre-MP
4	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PC163 SE074681K80 ( S CER CAP 680P 50V K X7R)	04/01/07	Pre-MP
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